



GT-21-475

VersaLink Bridge

High Speed Characterization Report for Differential Applications



Revision History

Rev	Date	Approved	Description
A	4/15/2021	L. Blackwell / B. Samowitz	Initial Release
B	10/6/2025	L. Blackwell	Added link to S-parameter app note



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1. Introduction

This document contains results from testing that was performed to evaluate the high-frequency electrical performance of the Glenair VersaLink Bridge in differential signaling applications. This report outlines frequency domain performance metrics such as insertion loss (IL) and return loss (RL) as well as time-domain performance metrics including impedance and eye diagrams.

For S-Parameter models of the results shown in this test report, refer to [AN0015](#).

2. Product Overview

The Glenair VersaLink Bridge is a high-density, micro-form factor twinax connector / jumper assembly used to bridge the gap between point A and point B on the board (such as between two SML integrated circuit chips) with better signal integrity than native board traces can ever deliver. VersaLink Bridge is equally capable of dramatically reducing insertion loss and signal latencies for data traffic between an ASIC and the I/O.

The VersaLink Bridge, when used as a PCB fly-over connection, provides a significantly lower loss signal path than a conventional PCB microstrip. The Glenair application note AN0011, *Improving Insertion Loss Budgets by using VersaLink Bridge*, describes in detail the advantage of employing the VersaLink Bridge.

3. Test Setup

This section details the test assemblies, test PCBs and equipment used to perform the high-speed characterization. All measurements were taken using a Tektronix DSA8300 Digital Serial Analyzer and a Keysight N5227B PNA network analyzer which were connected to SMA-launch test fixture PCBs designed specifically for this testing.

3.1. Test Assemblies

Two VersaLink Bridge cable assemblies were tested. Each VersaLink Bridge cable plug (853-064-1) was terminated to two six-inch pieces of PE-SR047F with an SMA jack.

A photograph of a representative test cable is presented in Figure 1.

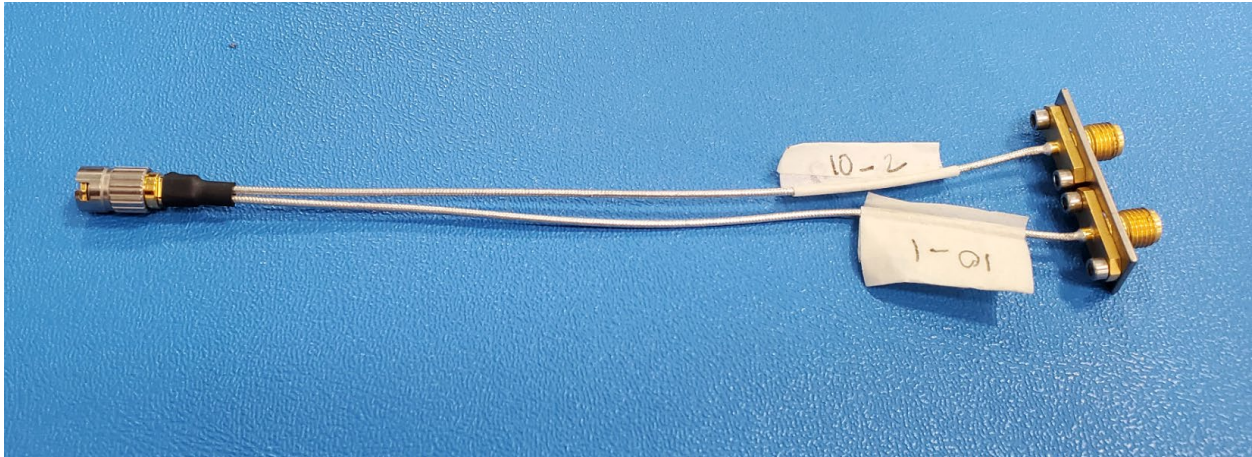


Figure 1. VersaLink Bridge Cable Assembly

3.2. Test Fixtures

3.2.1. Test PCBs

A test fixture PCB set utilizing edge-launch SMA connectors was designed for the high-speed tests. Each set consisted of a VersaLink Bridge to SMA board and a calibration board. One test set used a straight VersaLink PCB-mount connector, part number 853-065. The other set used right-angle VersaLink Bridge PCB-mount connector, part number 853-067. Photographs of the test boards are seen in the following two figures.

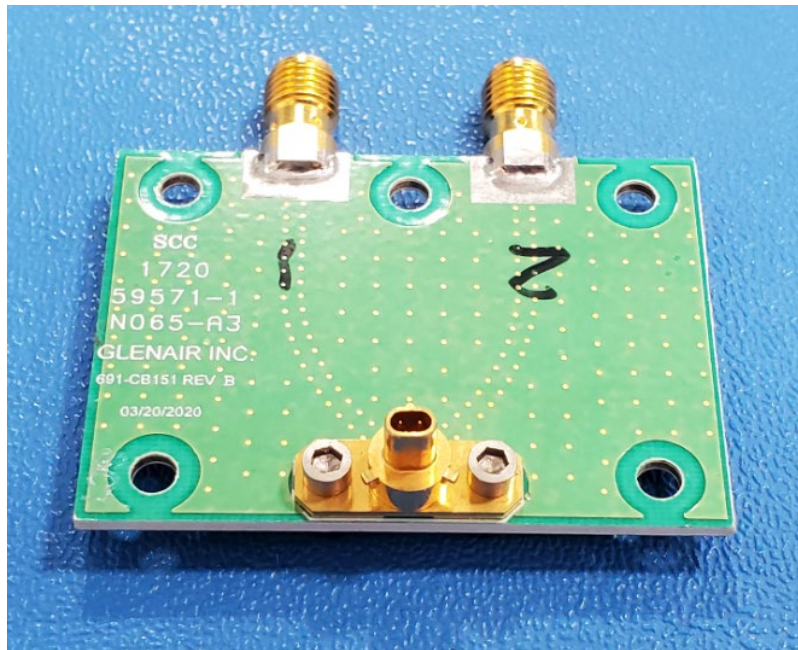


Figure 2. VersaLink Bridge Straight Test PCB

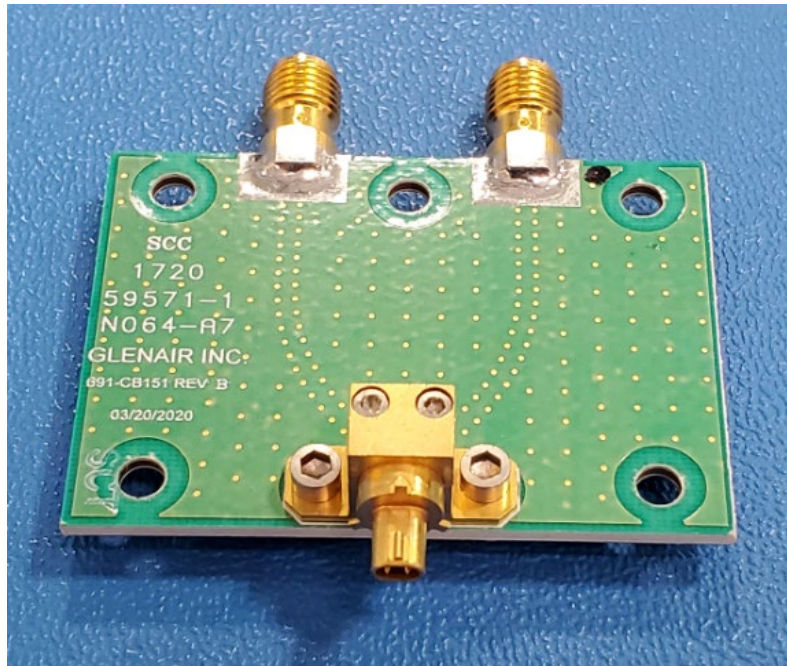


Figure 3. VersaLink Bridge Right-Angle Test PCB

The board sets were manufactured as a single panel and separated into individual test boards to give consistent signal characteristics.

3.3. Test Setup

Figure 4 shows test cabling connectivity for both the straight and right-angle VersaLink Bridge Test PCBs.

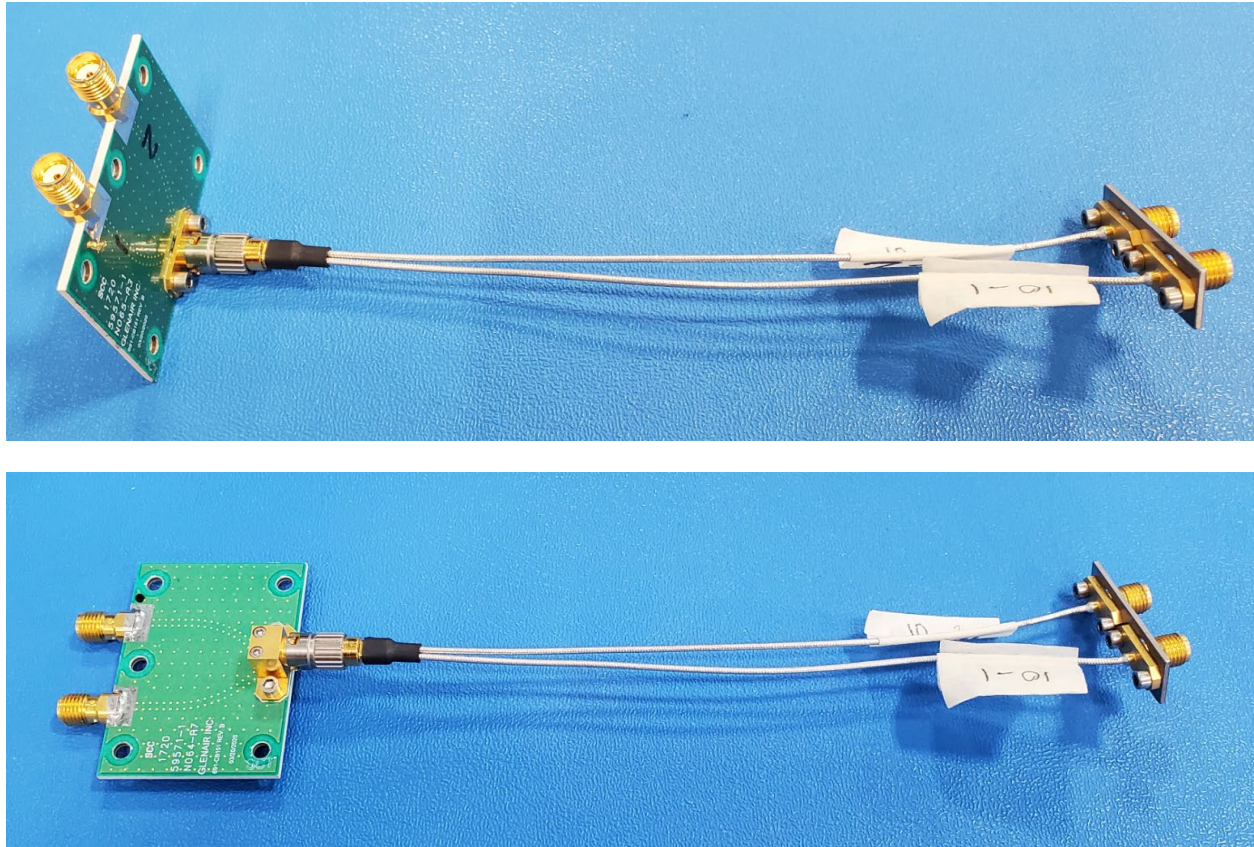


Figure 4. VersaLink Bridge Test Setup Connectivity

4. 2x-Thru Fixture Performance

This section includes both frequency and time domain results of the 2x-thru PCB and 2x-thru cable assembly used to extract the VersaLink Bridge electrical characteristics from the overall measured DUT/fixturing data.

4.1. Frequency Domain Analysis

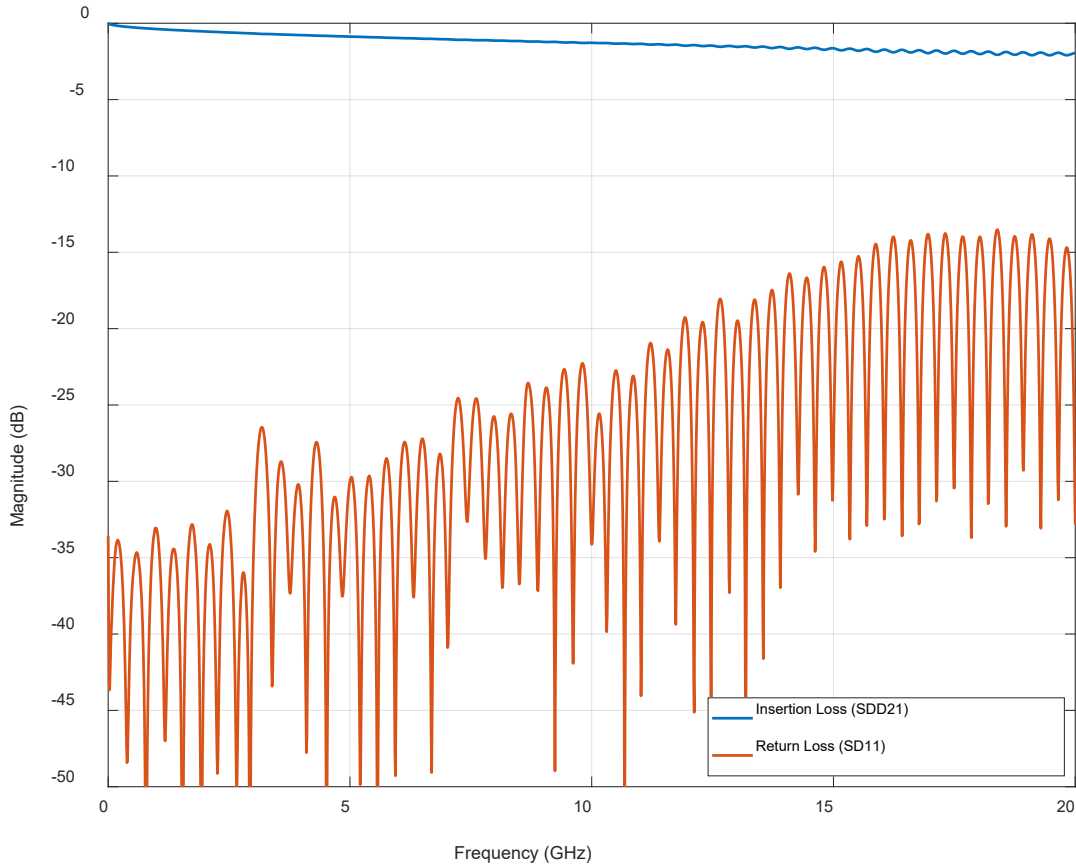


Figure 5. Straight VersaLink Bridge 2x-Thru Cable Assembly Response

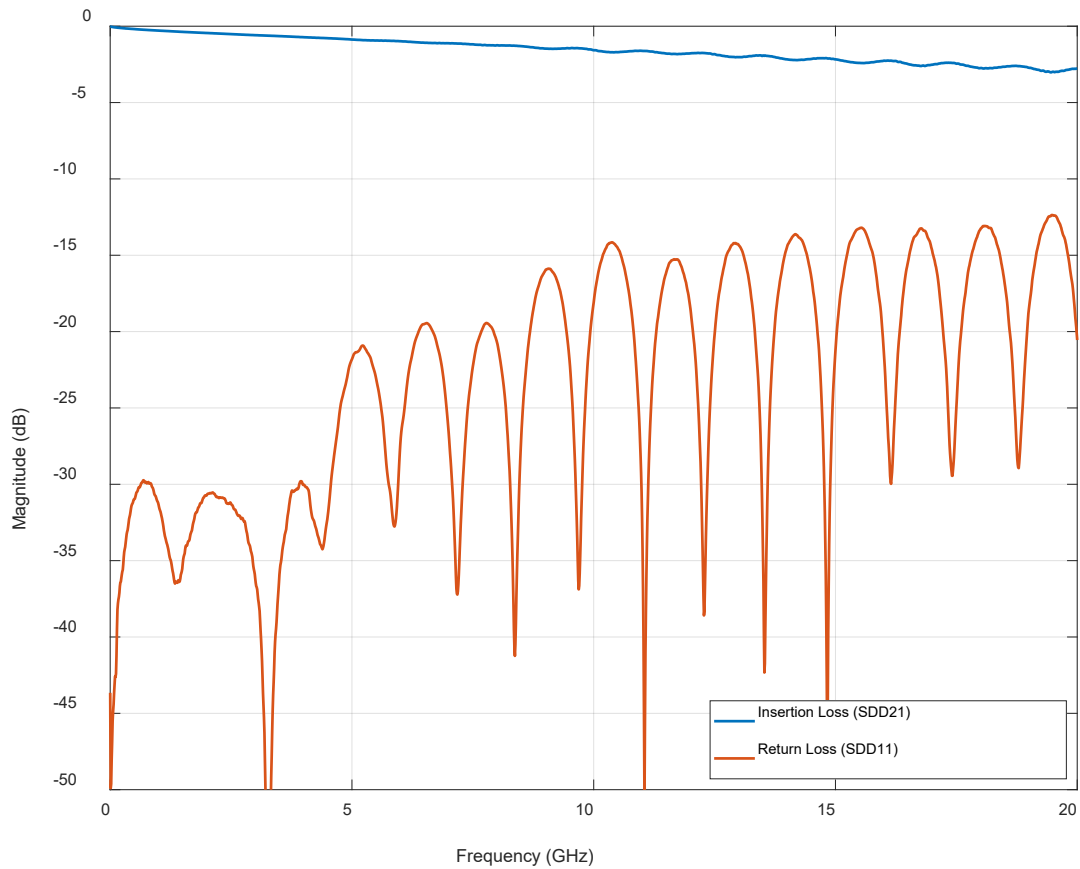


Figure 6. Straight VersaLink Bridge 2x-Thru PCB Response

5. Straight VersaLink Bridge Performance

This section includes both frequency and time domain results. Test fixture PCB and test cabling loss have been de-embedded to show the performance of the assembly only.

5.1. Frequency Domain Analysis

5.1.1. Straight VersaLink Bridge Insertion Loss

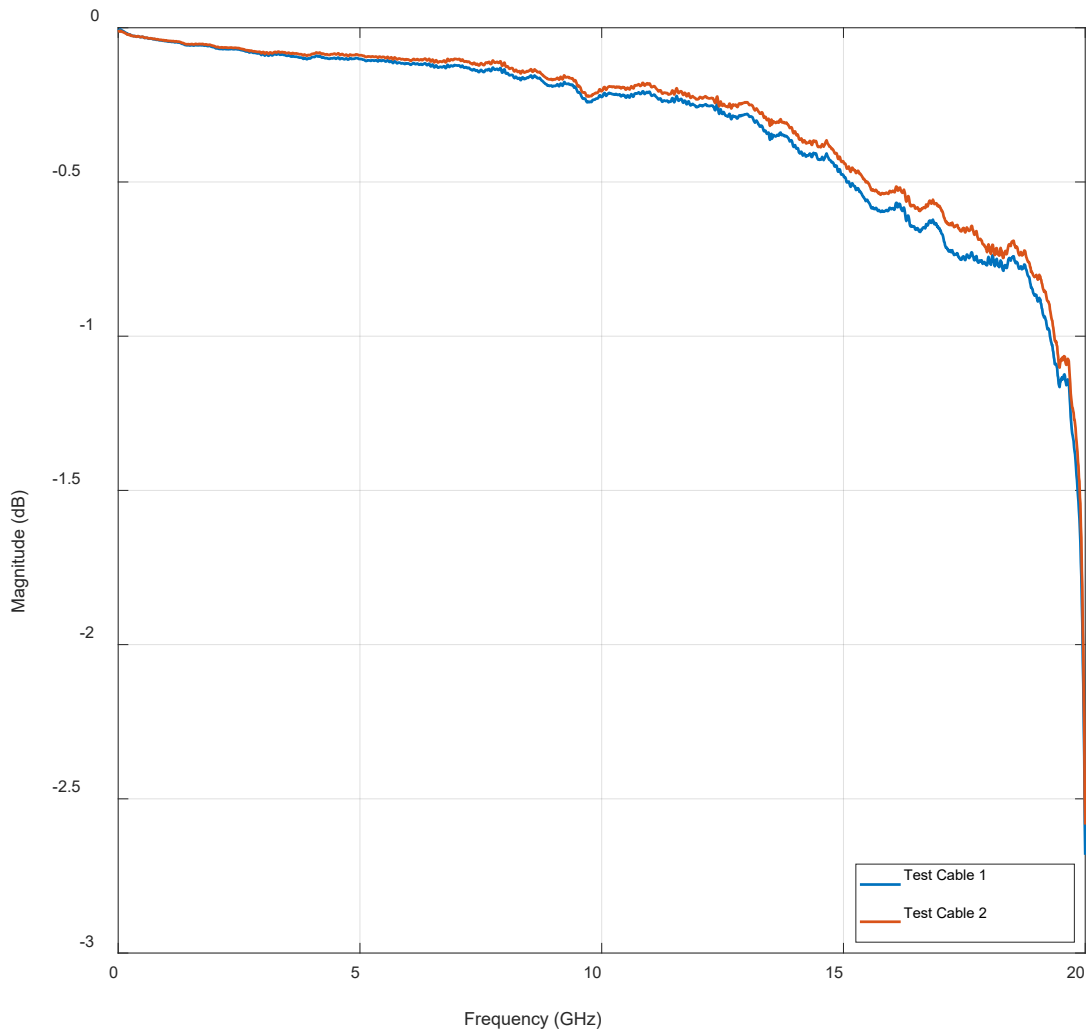


Figure 7. Straight VersaLink Bridge Insertion Loss

5.1.2. Straight VersaLink Bridge Return Loss

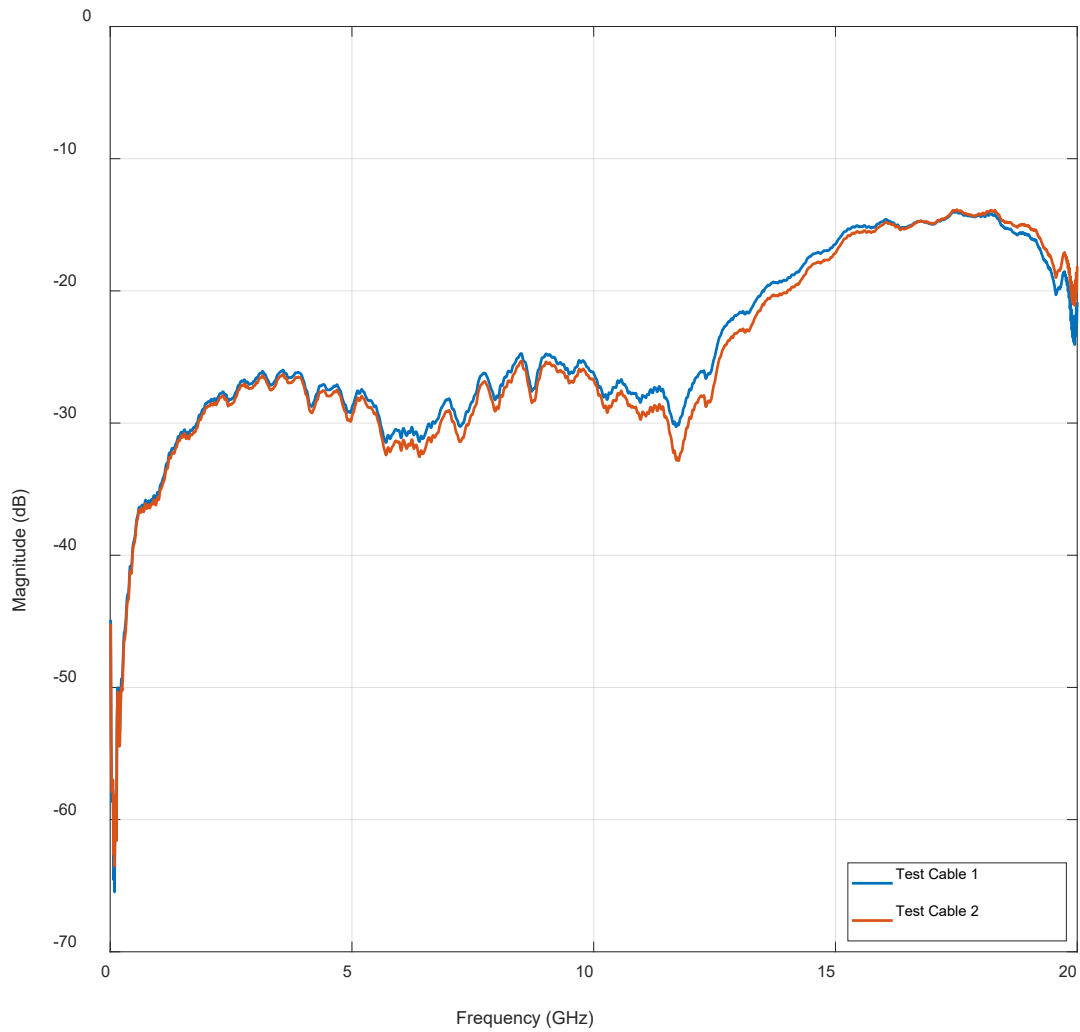


Figure 8. Straight VersaLink Bridge Return Loss

5.1.3. Straight VersaLink Bridge Bandwidth

The bandwidth of the Straight VersaLink Bridge can be drawn from Figure 9 by noting the frequency where the difference between the insertion loss and return loss is 3dB.

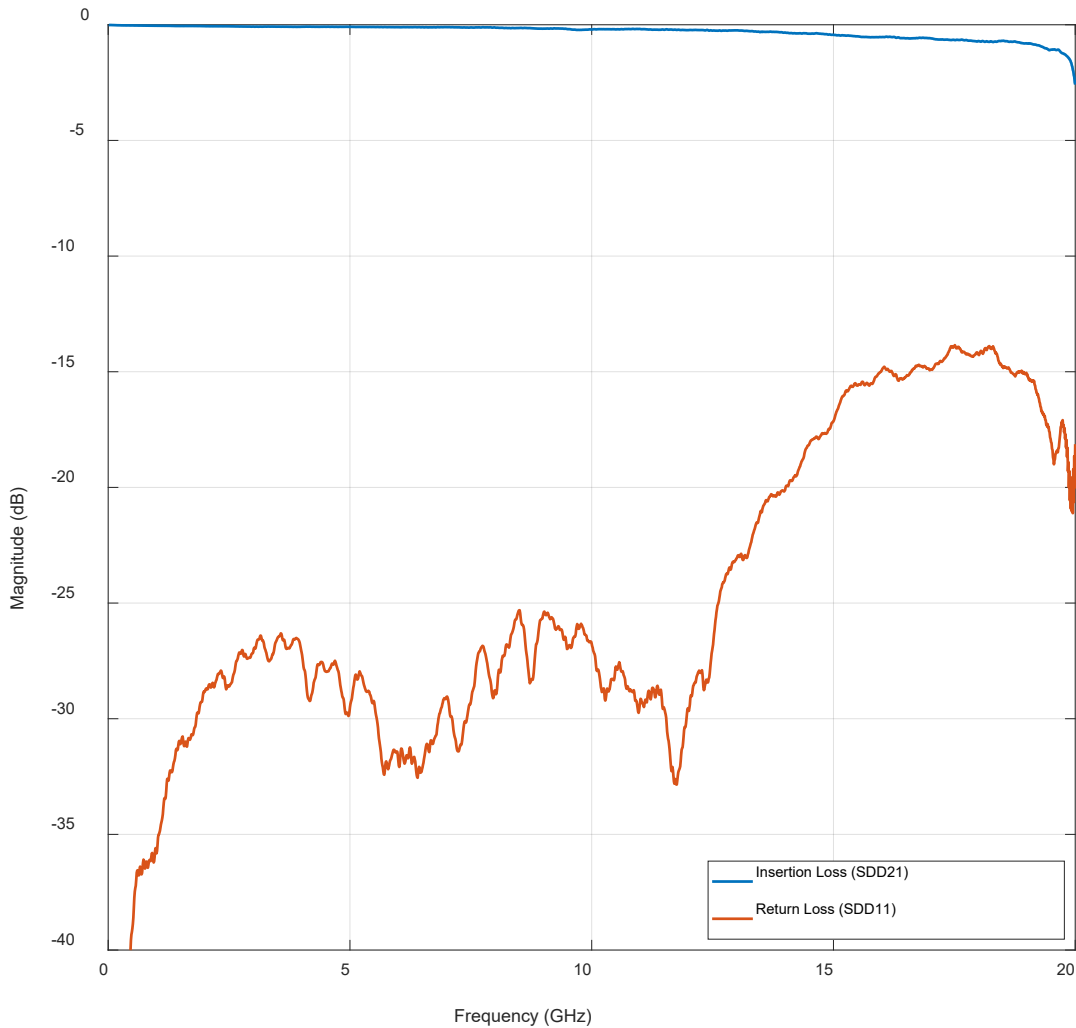


Figure 9. Straight VersaLink Bridge Bandwidth

In this manner, the bandwidth is found to be >20Ghz.

5.1.4. Straight VersaLink Bridge VSWR

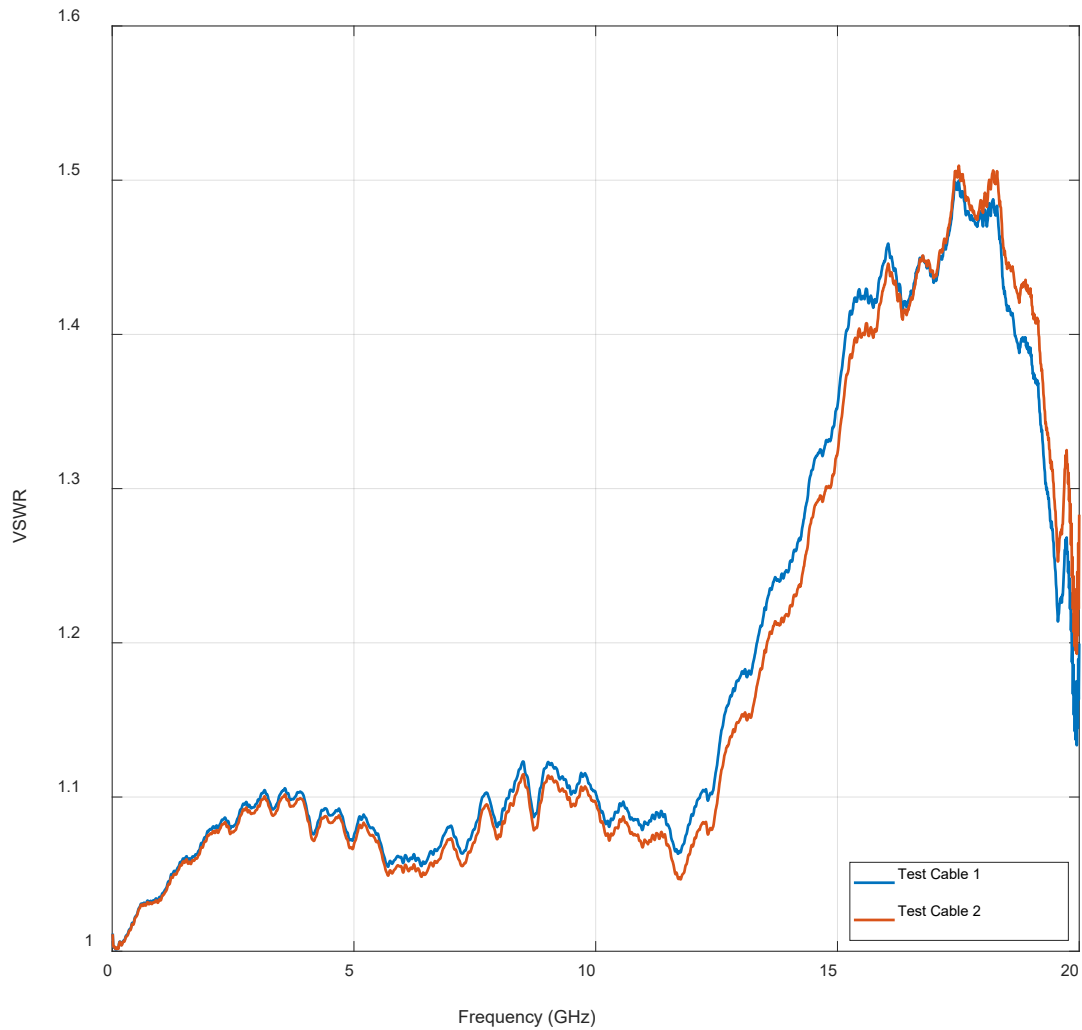


Figure 10. Straight VersaLink Bridge VSWR

5.2. Straight VersaLink Bridge Time Domain Analysis

5.2.1. Straight VersaLink Bridge TDR

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 20% to 80% of the signal's rising edge. Rise times of 25ps, 35ps, 50ps, and 100ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
25	14
35	10
50	7
100	3.5

Table 1. Bandwidth to Rise Time Relationship

The assembly's physical features and resulting impedance discontinuities are labeled in each plot.

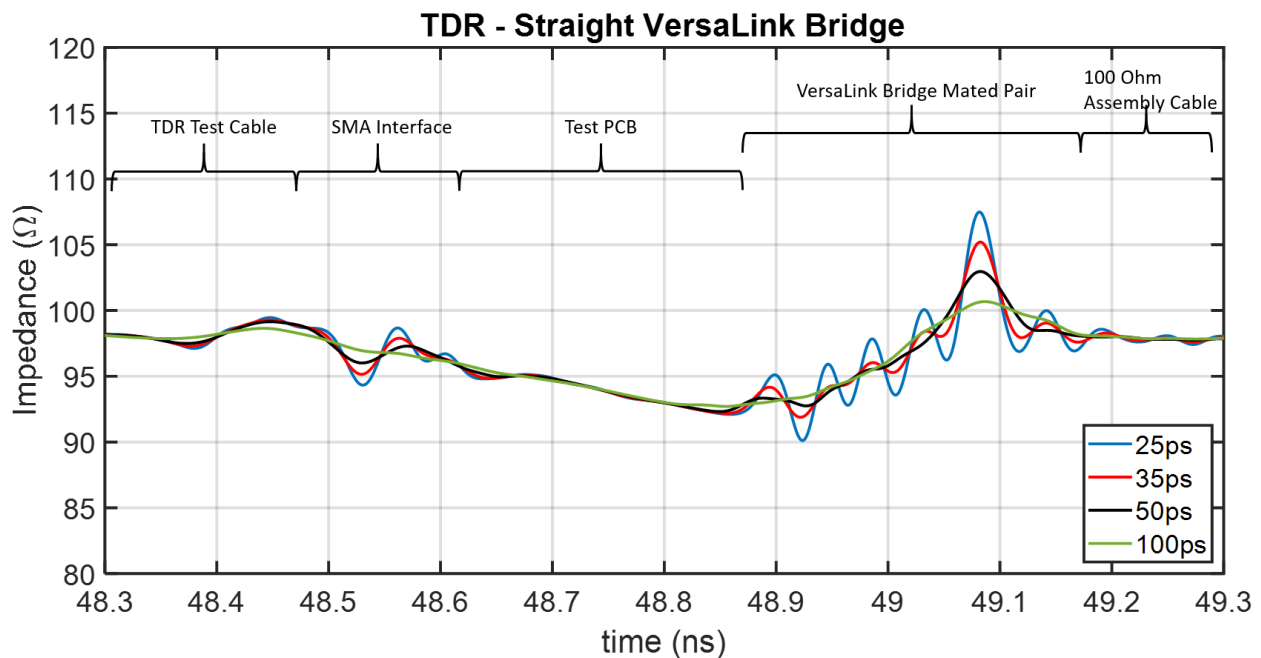


Figure 11. TDR – Straight VersaLink Bridge

5.2.2. Straight VersaLink Bridge Eye Diagrams

The S-parameter data obtained from the Keysight N5227B PNA measurements were used to generate statistical eye diagrams for bit rates of 5Gbps, 10Gbps, 20Gbps, and 28Gbps and are presented in the following four figures.

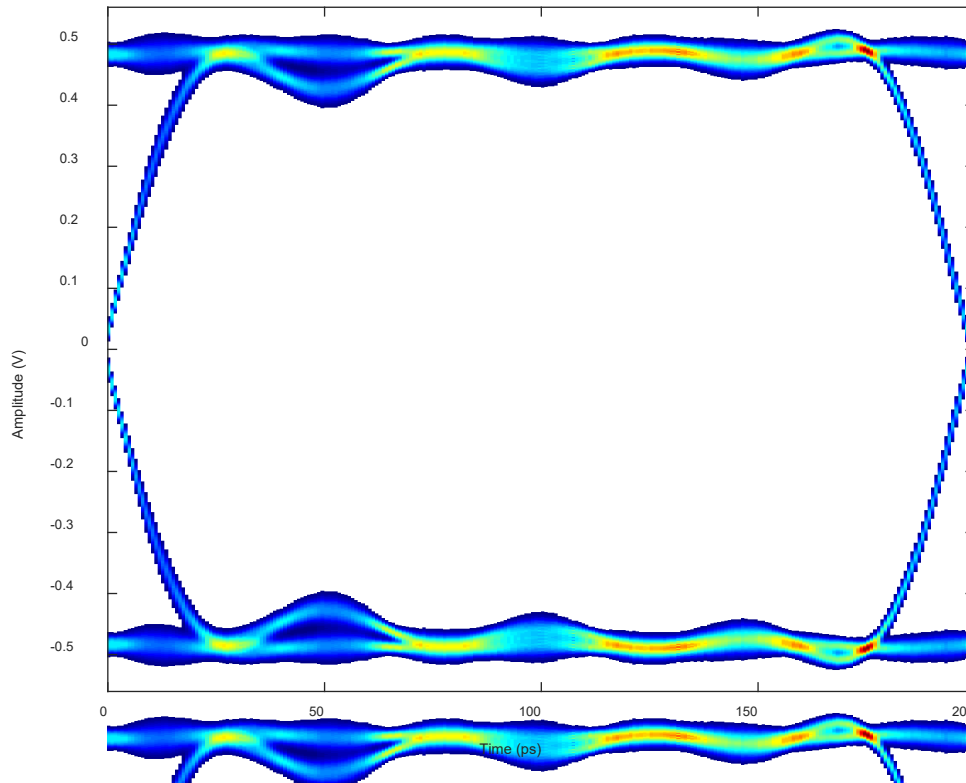


Figure 12. Eye diagram of Straight VersaLink Bridge at 5Gbps

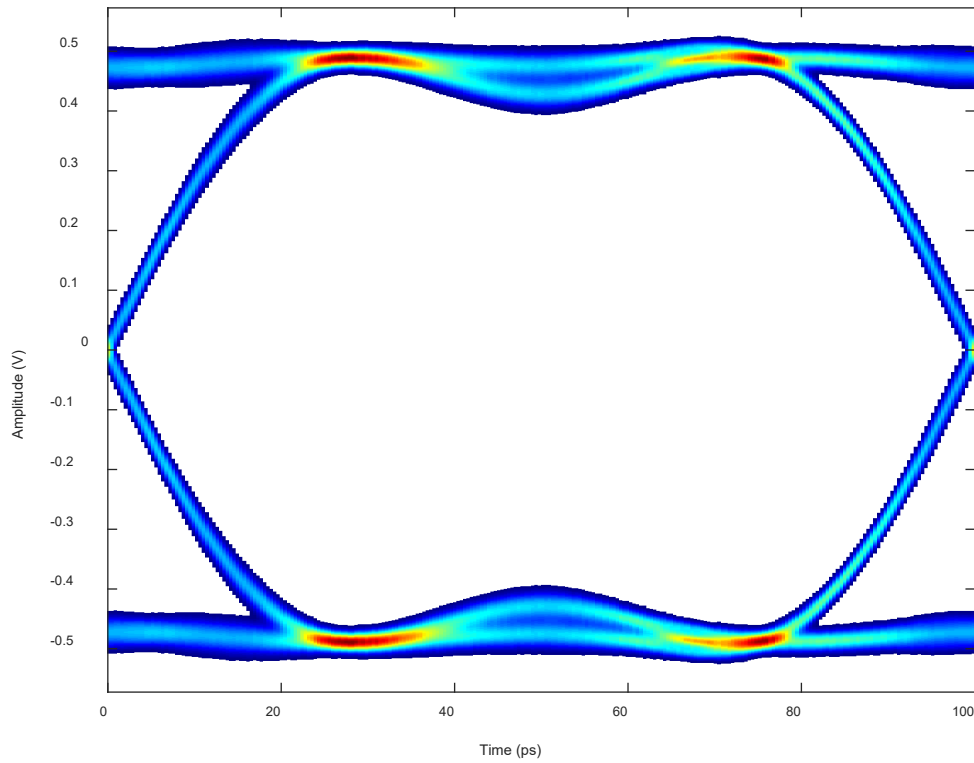


Figure 13. Eye diagram of Straight VersaLink Bridge at 10Gbps

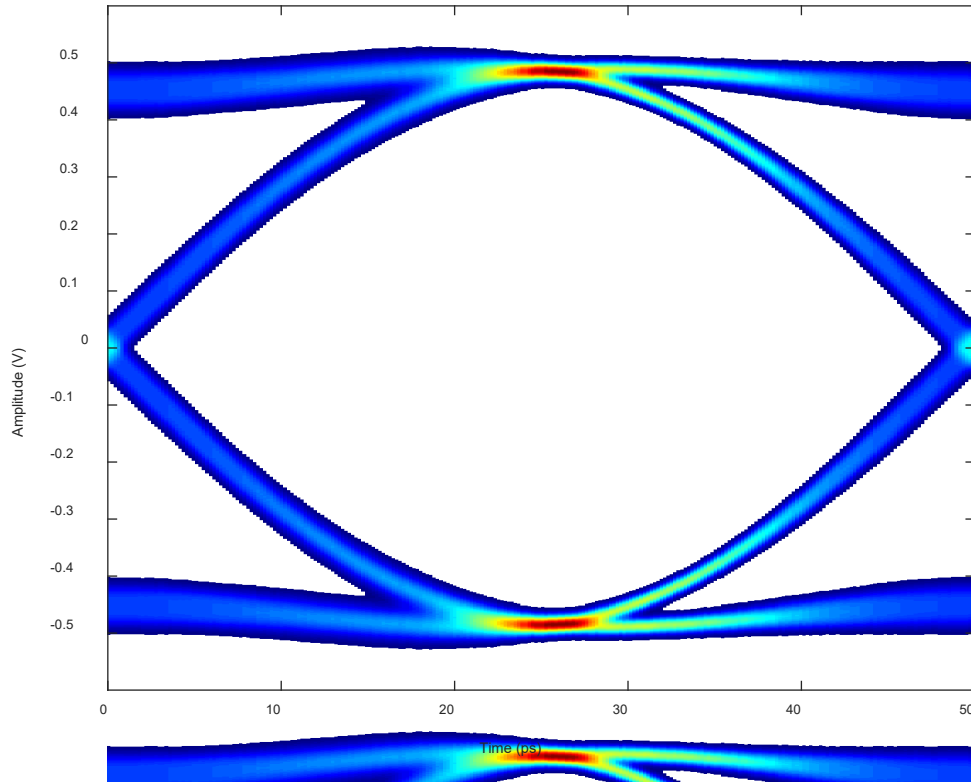


Figure 14. Eye diagram of Straight VersaLink Bridge at 20Gbps

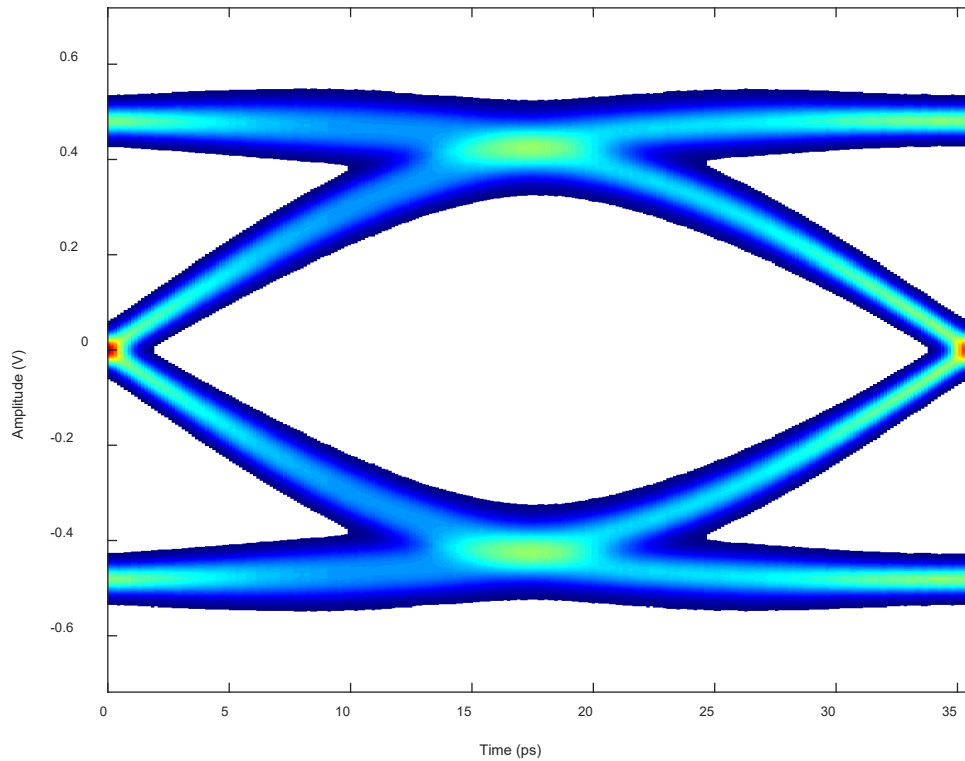


Figure 15. Eye diagram of Straight VersaLink Bridge at 28Gbps

6. Right-Angle VersaLink Bridge Performance Summary

This section includes both frequency and time domain results. Test fixture PCB and test cabling loss have been de-embedded to show the performance of the assembly only.

6.1. Frequency Domain Analysis

6.1.1. Right-Angle VersaLink Bridge Insertion Loss

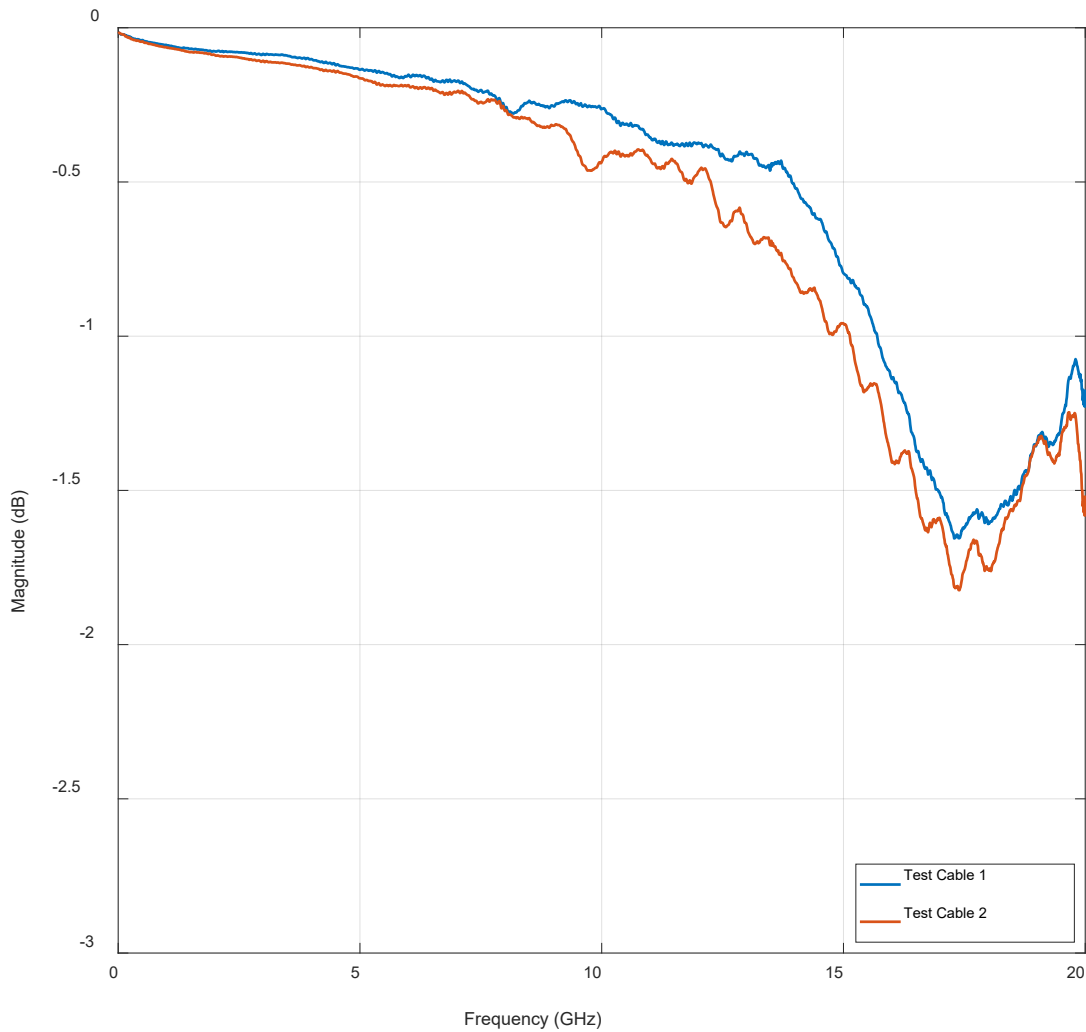


Figure 16. Right-Angle VersaLink Bridge Insertion Loss

6.1.2. Right-Angle VersaLink Bridge Return Loss

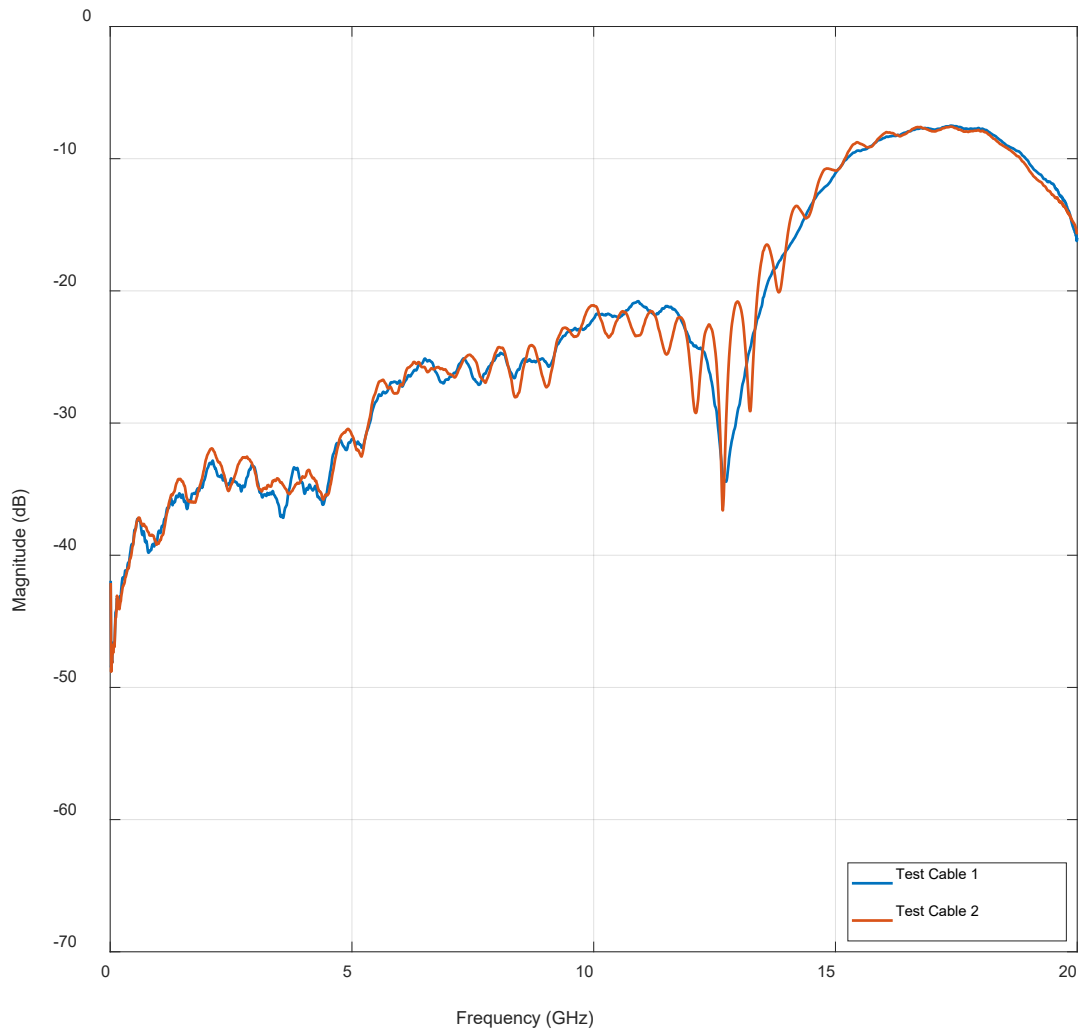


Figure 17. Right-Angle VersaLink Bridge Return Loss

6.1.3. Right-Angle VersaLink Bridge Bandwidth

The bandwidth of the Right-Angle VersaLink Bridge can be drawn from Figure 18 by noting the frequency where the difference between the insertion loss and return loss is 3dB.

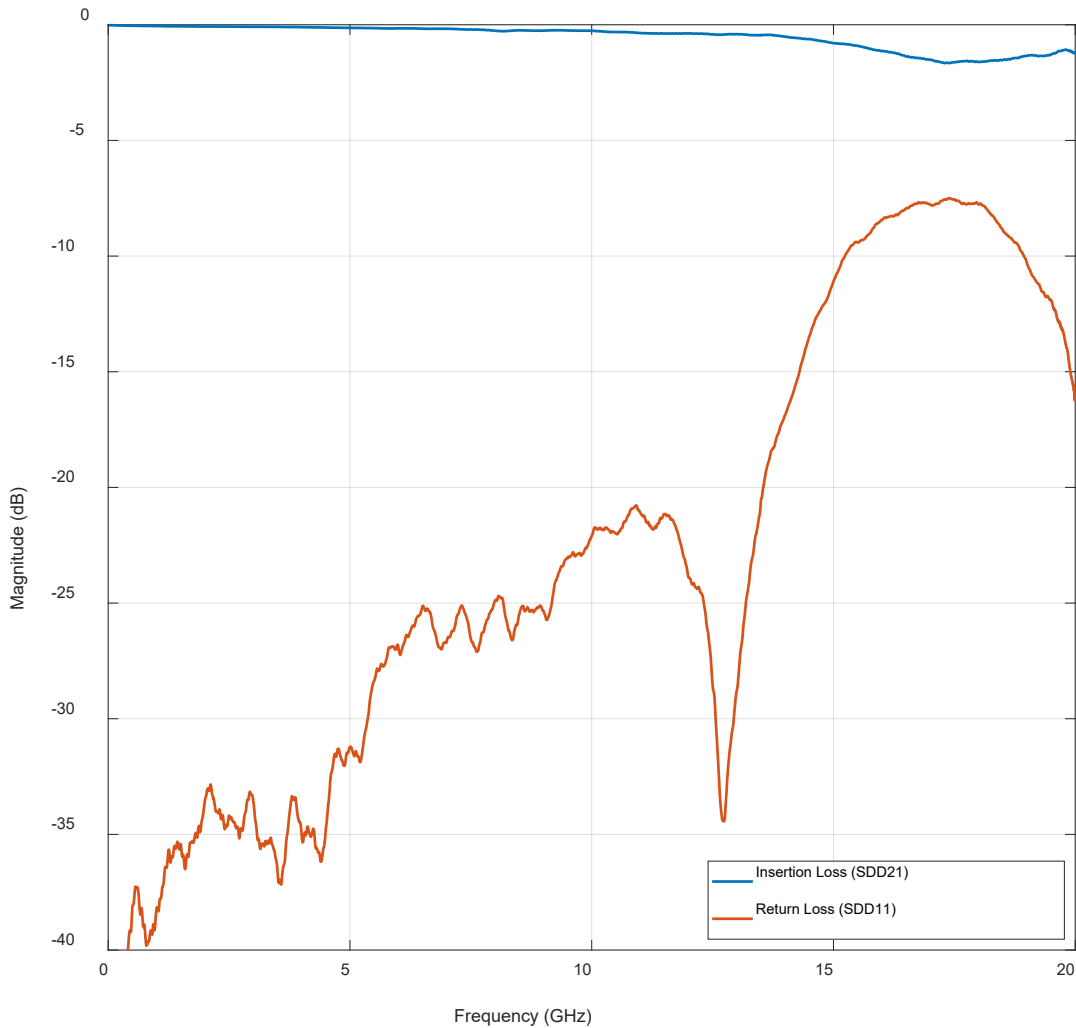


Figure 18. Right-Angle VersaLink Bandwidth

In this manner, the bandwidth is found to be >20Ghz.

6.1.4. Right-Angle VersaLink Bridge VSWR

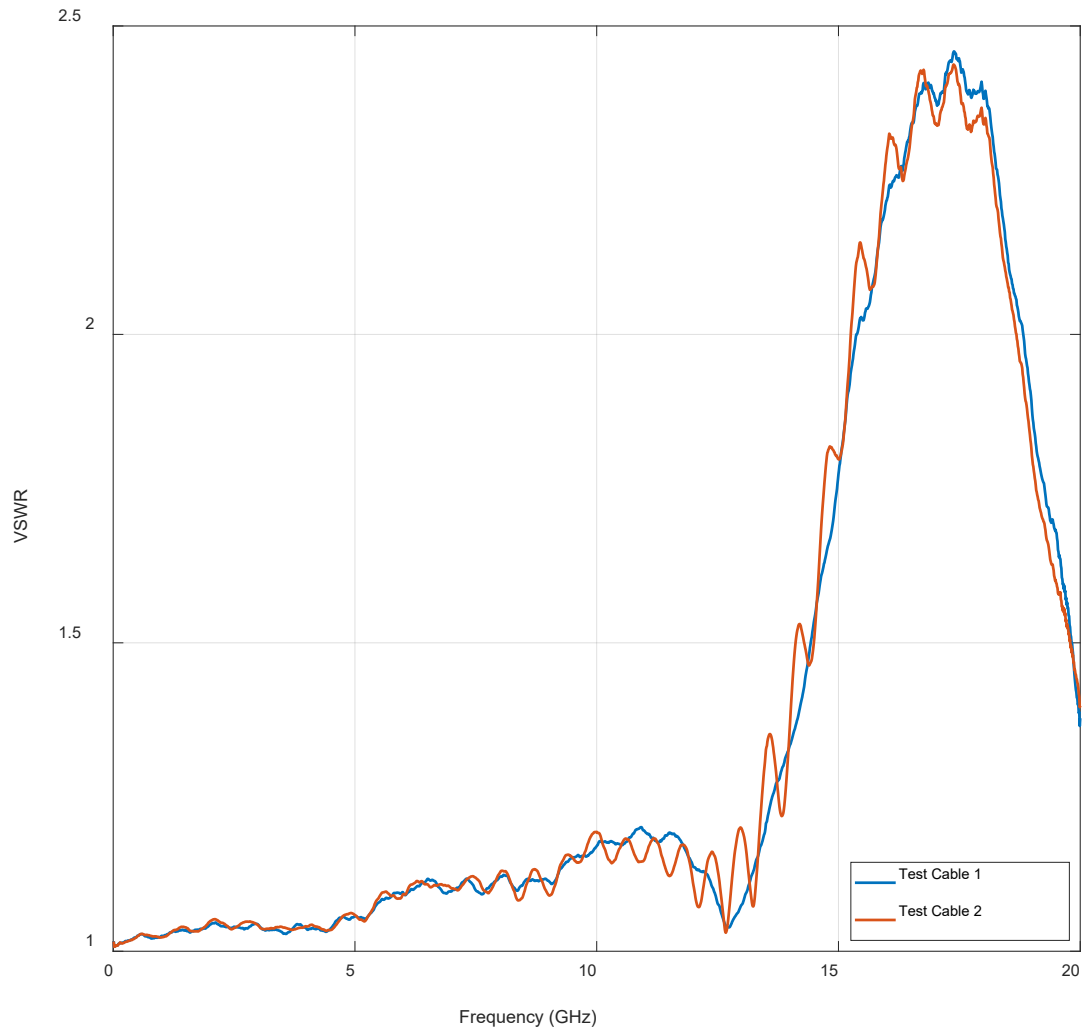


Figure 19. Right-Angle VersaLink Bridge VSWR

6.2. Right-Angle VersaLink Bridge Time Domain Analysis

6.2.1. Right-Angle VersaLink Bridge TDR

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 20% to 80% of the signal's rising edge. Rise times of 25ps, 35ps, 50ps, and 100ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
25	14
35	10
50	7
100	3.5

Table 1. Bandwidth to Rise Time Relationship

The assembly's physical features and resulting impedance discontinuities are labeled in each plot.

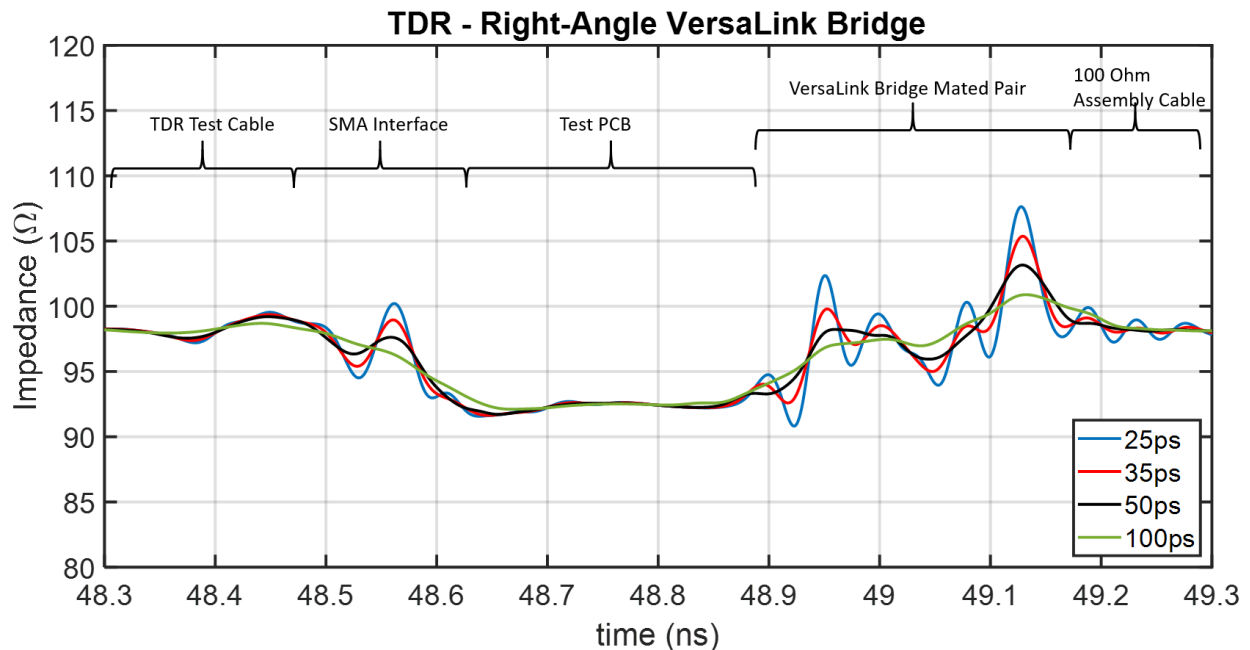


Figure 20. TDR – Right-Angle VersaLink Bridge

6.2.2. Right-Angle VersaLink Bridge Eye Diagrams

As with the Straight VersaLink Bridge, the S-parameter data obtained from the Keysight N5227B PNA measurements were used to generate statistical eye diagrams for bit rates of 5Gbps, 10Gbps, 20Gbps, and 28Gbps and are presented in the following four figures.

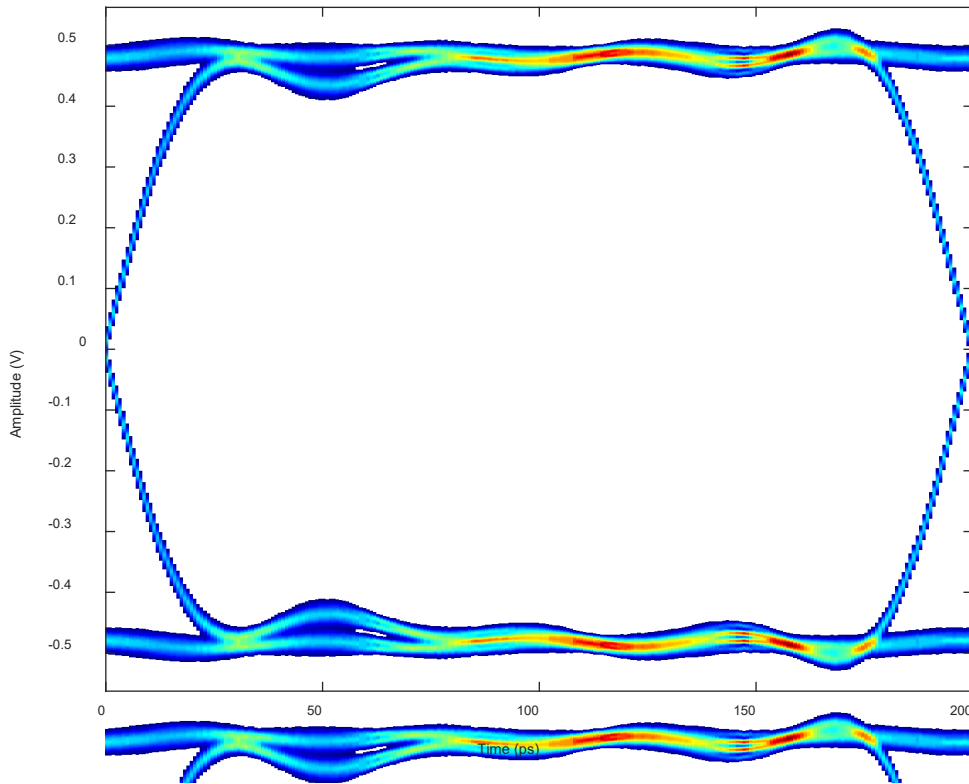


Figure 21. Eye diagram of Right-Angle VersaLink Bridge at 5Gbps

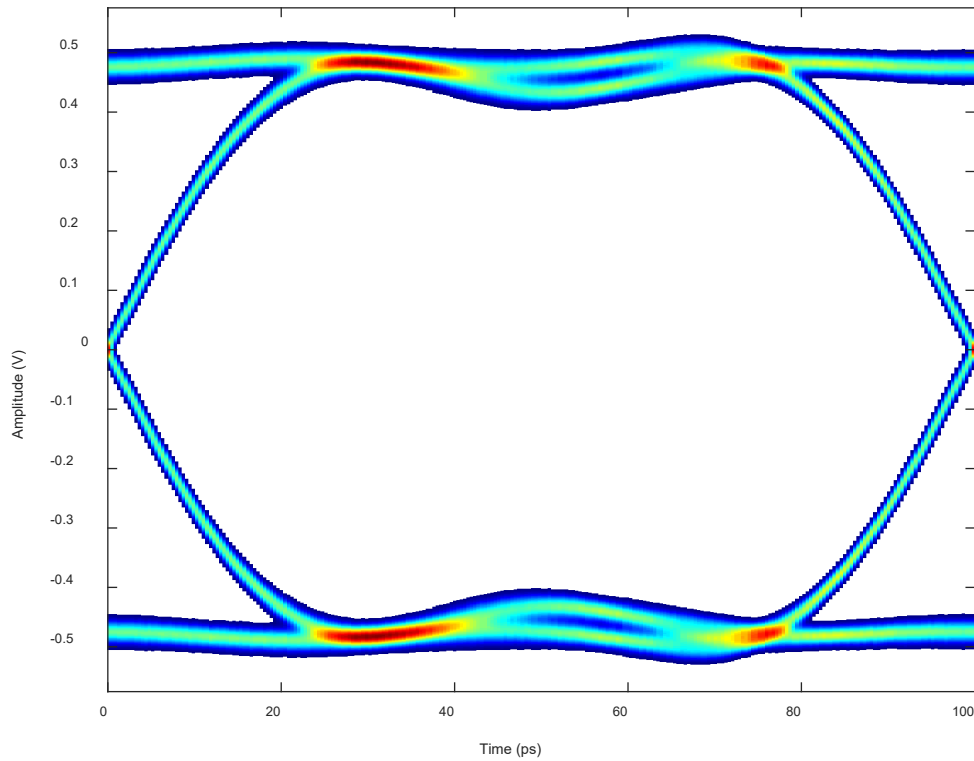


Figure 22. Eye diagram of Right-Angle VersaLink Bridge at 10Gbps

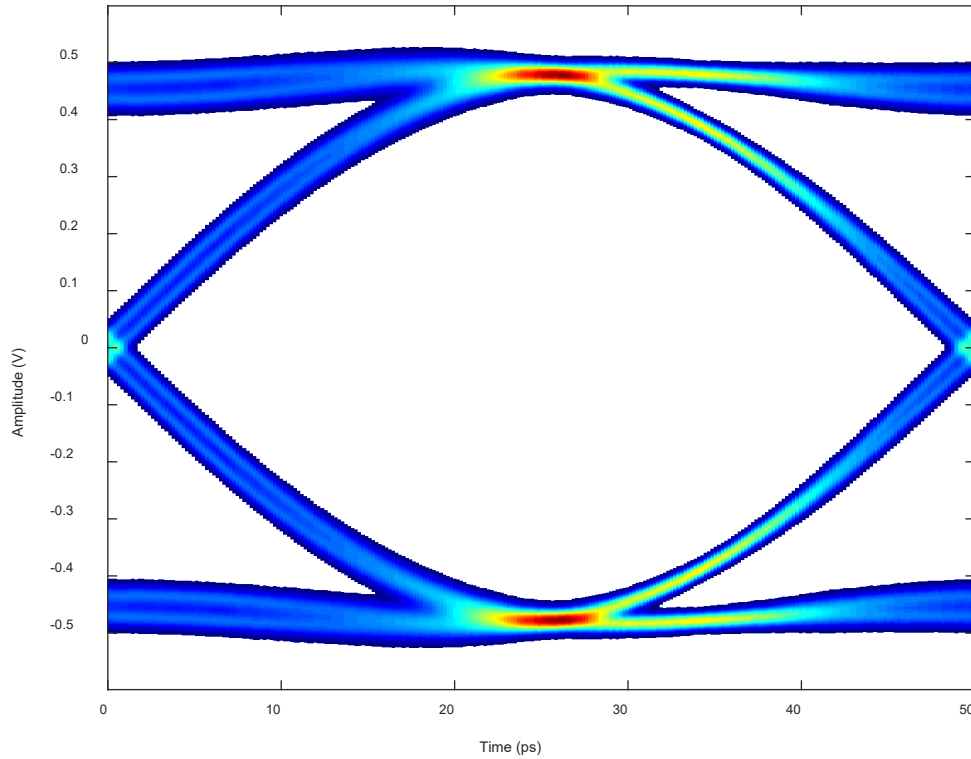


Figure 23. Eye diagram of Right-Angle VersaLink Bridge at 20Gbps

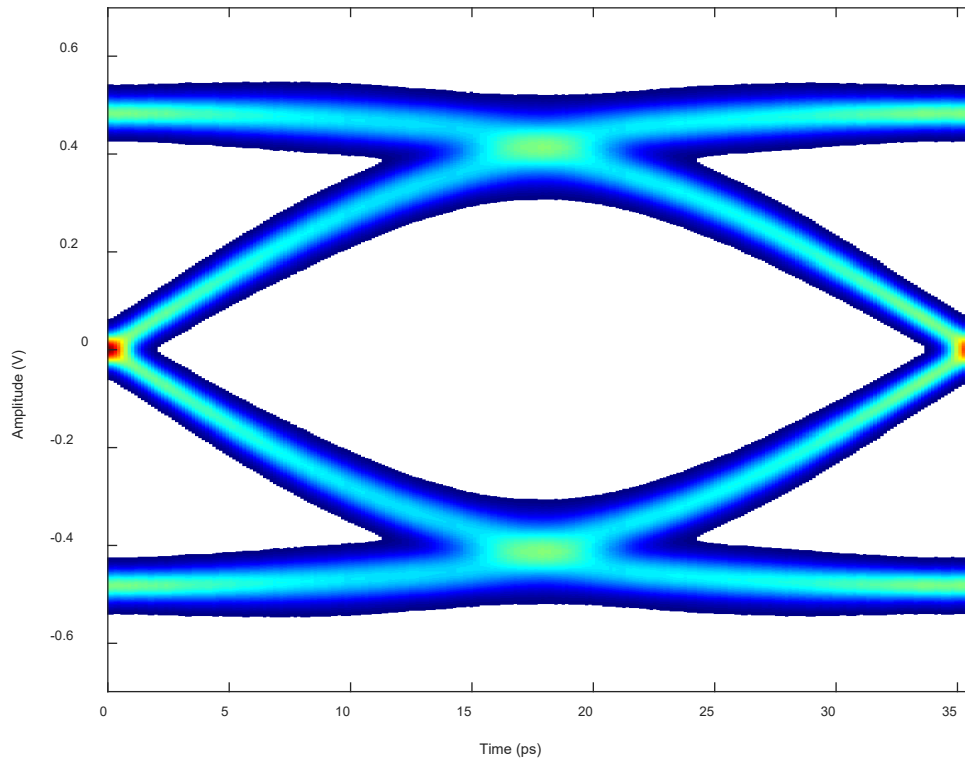


Figure 24. Eye diagram of Right-Angle VersaLink Bridge at 28Gbps



Appendix A. Connector Drawings

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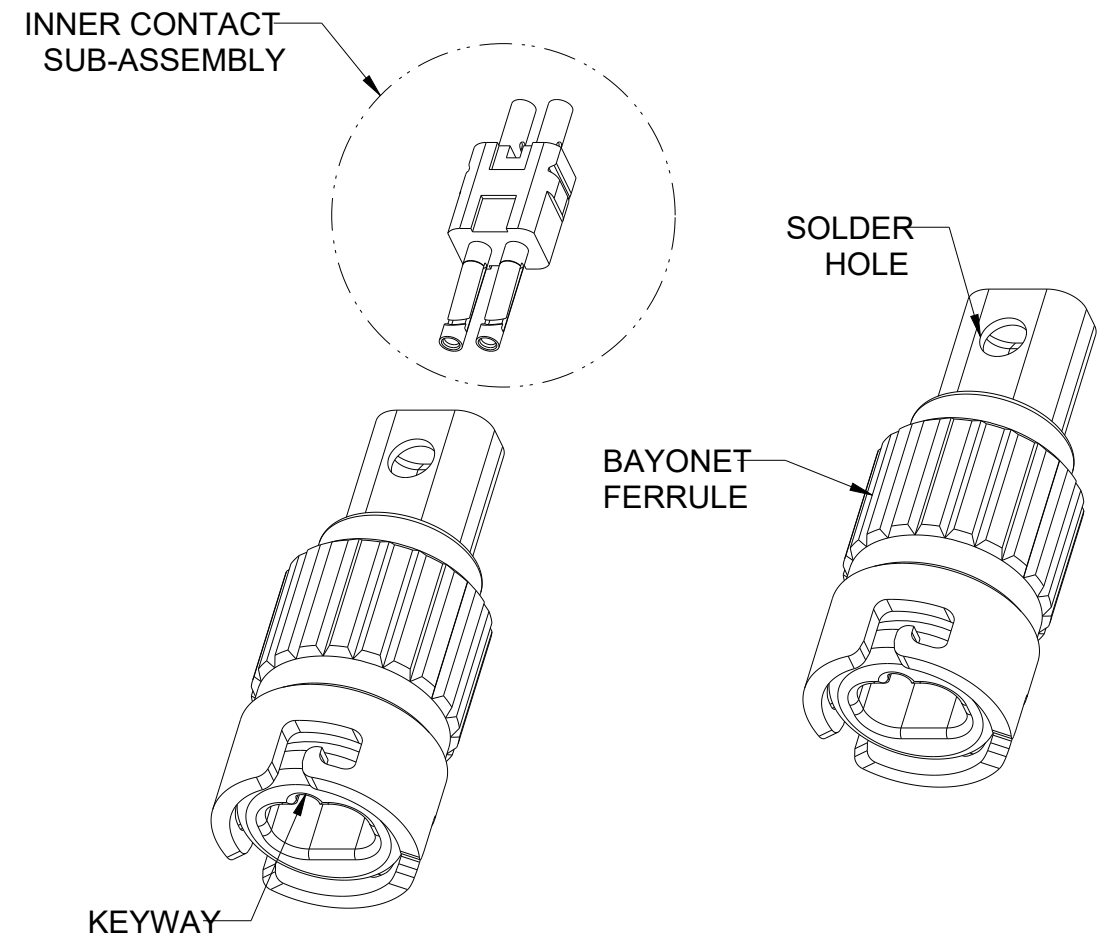
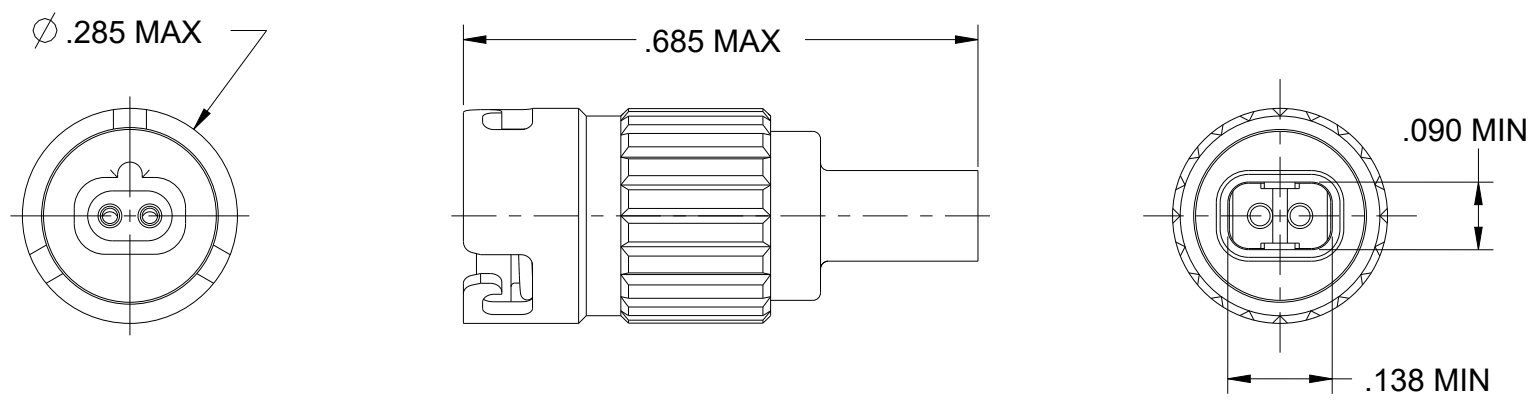
RECOMMENDED CABLES³

DASH NUMBER	CABLE P/N	CABLE CONSTRUCTION	WIRE GAUGE	MAX OVERALL SIZE	CRIMP DIE	ASSEMBLY INSTRUCTIONS
-01	963-043-26	TWINAX IN-LINE	26	.121 X .076	859-205-26	AI85153

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
1	PRELIMINARY	1/15/19	BNS
2	DASH NUMBER ADDED	11/21/19	BNS
3	TOOLING UPDATED	5/20/20	BNS
4	AI ADDED	6/22/20	BNS
5	LEADING 0 ADDED TO DASH NUMBER	7/15/21	BNS

853-064-01

PRODUCT CODE
 BASIC NO. _____
 DASH NO. _____



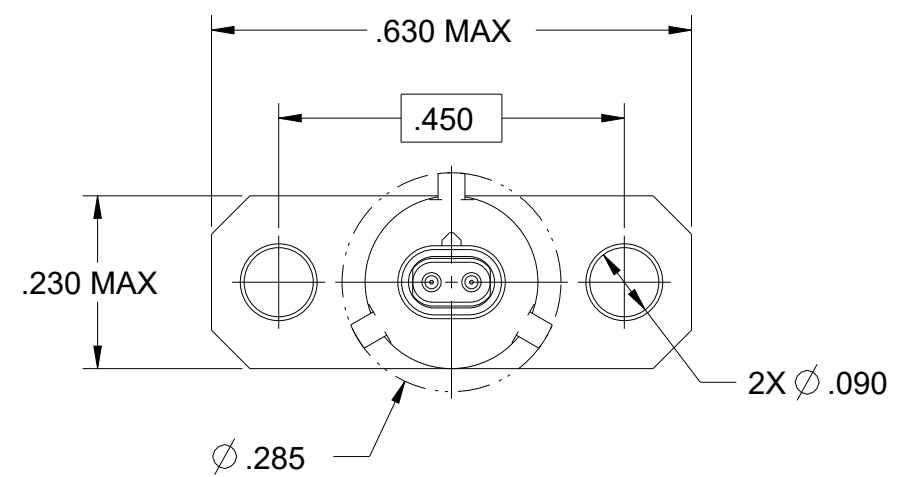
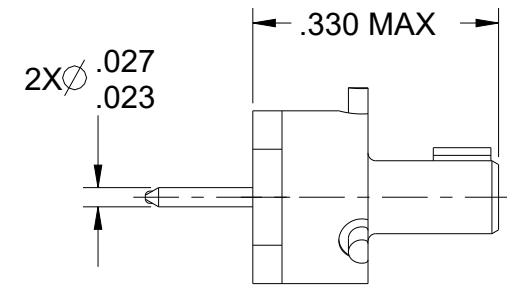
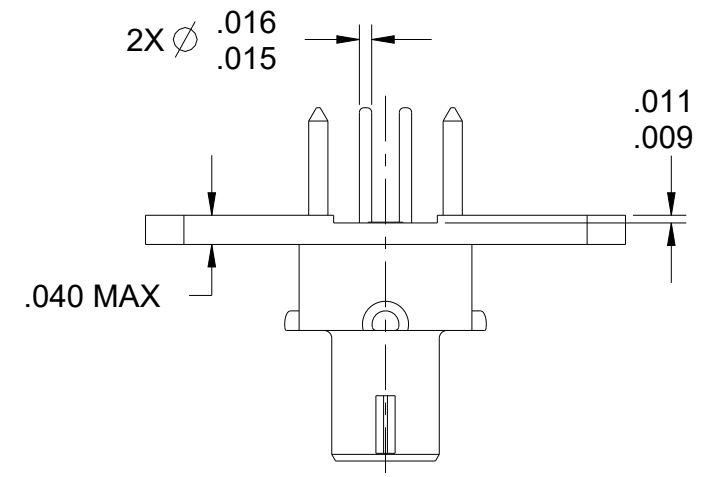
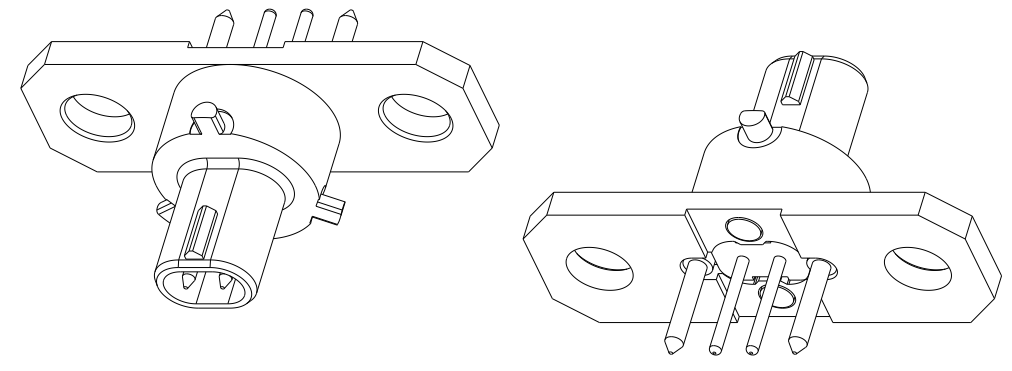
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- 4. CRIMP TOOL:
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 DIE: 859-205-XX
- 3. CONTACT FACTORY TO INQUIRE ABOUT USE WITH OTHER CABLES.
- 2. MATERIAL / FINISH:
 CONTACTS - COPPER ALLOY / GOLD
 INSULATORS - SUPERIOR RIGID DIELECTRIC / N.A.
 BODY - COPPER ALLOY / GOLD
 COUPLING NUT - COPPER ALLOY / ELECTROLESS NICKEL
 SPRING - STAINLESS STEEL / N.A.
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NOTES: UNLESS OTHERWISE SPECIFIED

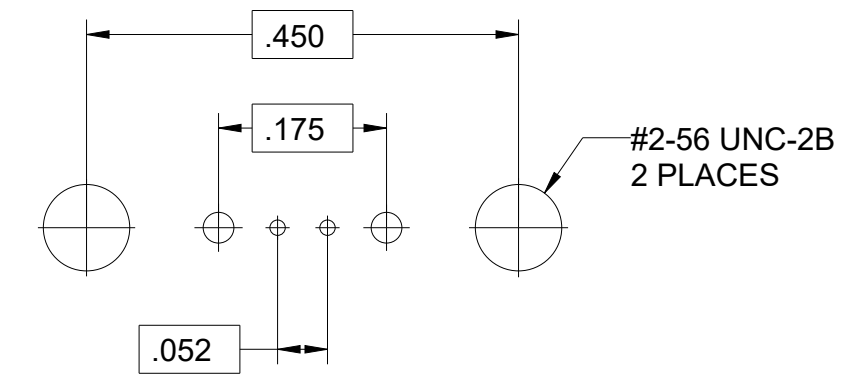
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	CHECK	BNS	1/15/19		
	ENGR	BNS	1/15/19		
TOLERANCES: FRACTIONS SYMMETRY ϕ RADI	<i>D. Brown</i> APPROVED		TITLE PLUG, BOARD, SOCKET BAYONET VERSALINK BRIDGE		
DECIMALS .X .XX .XXX .XXXX	<i>D. Brown</i> APPROVED				
ANGLES	DO NOT SCALE THIS DRAWING		RELEASE DATE	N/A	
B/F	N/A	P/C	853	ORIGINAL RELEASE DATE	N/A
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06324			B	853-064	5
SCALE: N/A			WEIGHT: N/A		SHEET 1 OF 1

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SYM	DESCRIPTION	DATE	APPROVED
1	PRELIMINARY	1/15/19	BNS
2	NOTES UPDATED	6/22/20	BNS



853-065-G-.140
 PRODUCT CODE
 BASIC NO.
 PC TAIL FINISH
 S = SOLDER DIPPED
 IN 63/37 TIN-LEAD
 G = GOLD PLATED
 PC TAIL LENGTH (IN): .140
 .110
 .080



PCB LAYOUT 5

5. MATES WITH 853-064.

4 SEE APPLICATION NOTE AN0005 FOR OPTIMAL PCB LAYOUT.

3. ELECTRICAL PARAMETERS:
 IMPEDANCE: 100 Ω
 DIELECTRIC WITHSTANDING VOLTAGE: 500 VRMS
 INSULATION RESISTANCE: 5000 MEGAOHMS MIN AT 200 VDC

2. MATERIAL / FINISH:
 CONTACTS - COPPER ALLOY / GOLD
 INSULATORS - SUPERIOR RIGID DIELECTRIC / N.A.
 BODY - COPPER ALLOY / GOLD

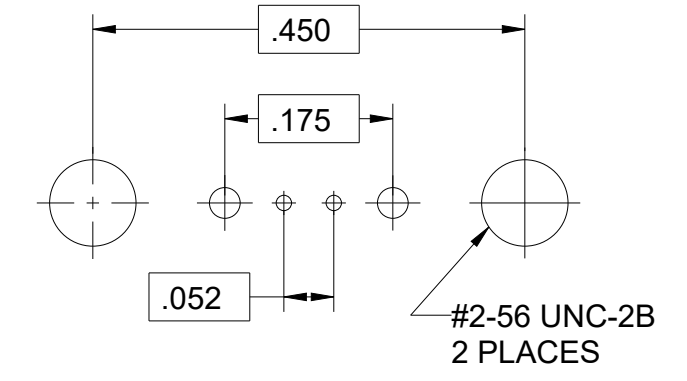
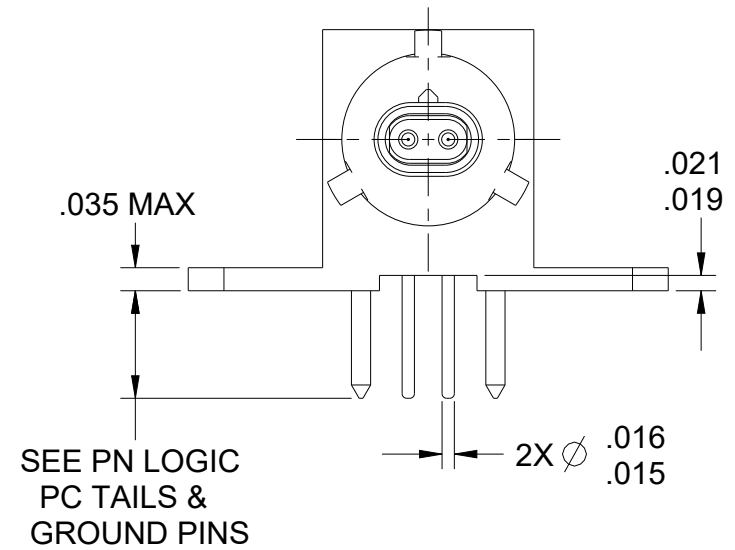
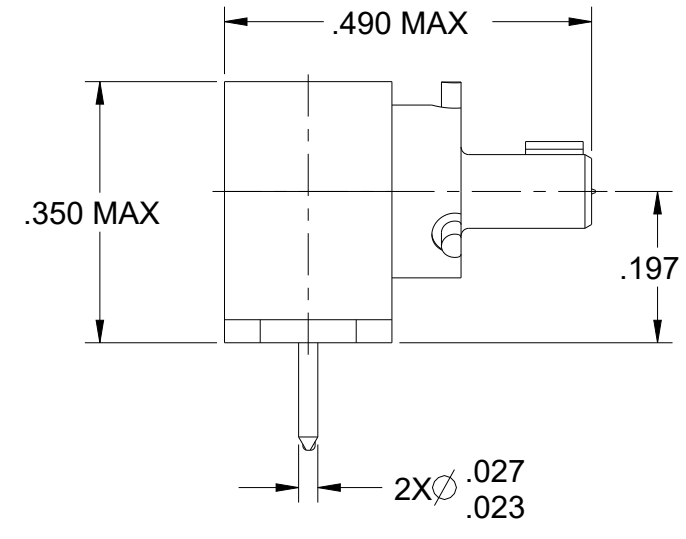
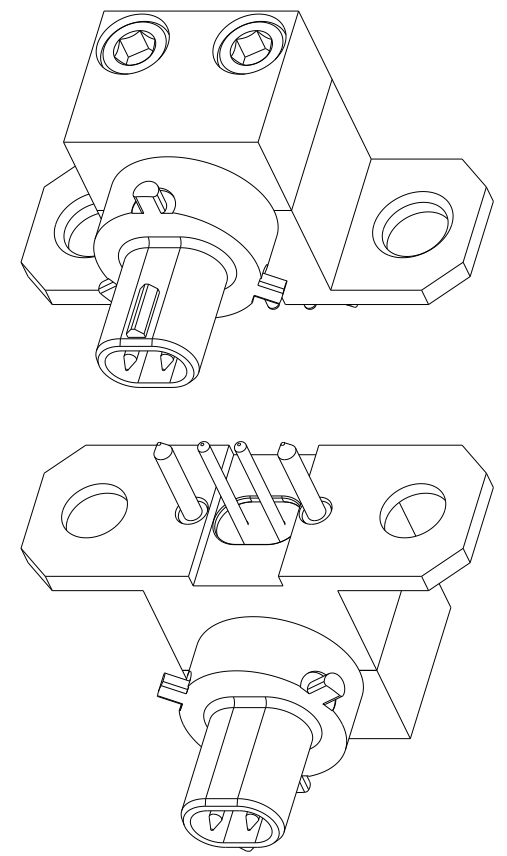
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NOTES: UNLESS OTHERWISE SPECIFIED

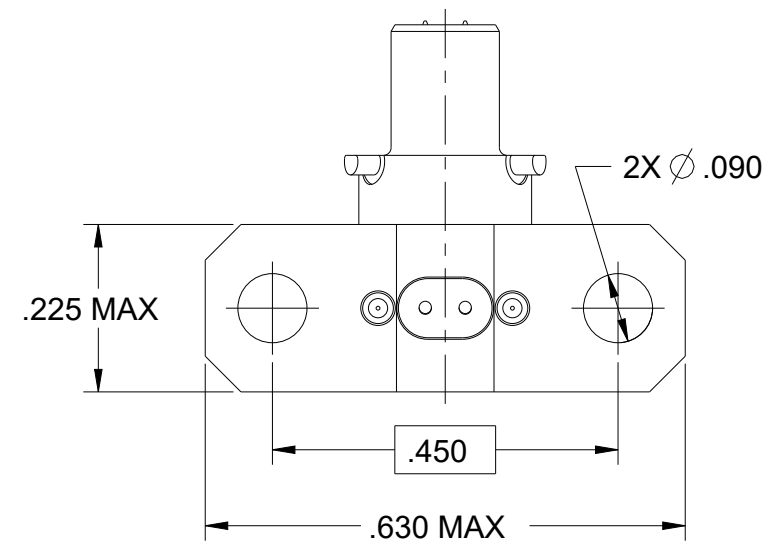
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				CHECK	BNS	1/15/19					
				ENGR	BNS	1/15/19					
TOLERANCES: FRACTIONS SYMMETRY \pm RADI				<i>D. Brown</i> APPROVED			TITLE JACK, BOARD, PIN VERTICAL, BAYONET VERSALINK BRIDGE				
DECIMALS .X .XX .XXX .XXXX				<i>D. Brown</i> APPROVED							
ANGLES							CODE IDENT. NO.	SIZE	DWG NO	REV	
DO NOT SCALE THIS DRAWING				RELEASE DATE			N/A	06324	B	853-065	2
B/F	N/A	P/C	853	ORIGINAL RELEASE DATE			N/A	SCALE: N/A		WEIGHT: N/A	SHEET 1 OF 1

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SYM	DESCRIPTION	DATE	APPROVED
1	PRELIMINARY	3/1/17	BNS
2	NOTES UPDATED	6/22/20	BNS



PCB LAYOUT 4



853-067-G-.140

PRODUCT CODE _____

BASIC NO. _____

PC TAIL FINISH _____

S = SOLDER DIPPED
IN 63/37 TIN-LEAD

G = GOLD PLATED

PC TAIL LENGTH (IN): .140
.110
.080

5. MATES WITH 853-064.

4 SEE APPLICATION NOTE AN0005 FOR OPTIMAL PCB LAYOUT.

3. ELECTRICAL PARAMETERS:
 IMPEDANCE: 100 Ω
 DIELECTRIC WITHSTANDING VOLTAGE: 500 VRMS
 INSULATION RESISTANCE: 5000 MEGAOHMS MIN AT 200 VDC

2. MATERIAL / FINISH:
 CONTACTS - COPPER ALLOY / GOLD
 INSULATORS - SUPERIOR RIGID DIELECTRIC / N.A.
 BODY - COPPER ALLOY / GOLD

1. VERSALINK COMPONENTS SHALL BE KITTED, BAGGED AND TAGGED WITH GLENAIR'S NAME, PART NUMBER AND DATE CODE.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DRAWN	BNS	3/1/17
		CHECK	BNS	3/1/17
		ENGR	BNS	3/1/17
TOLERANCES:		 APPROVED		
FRACTIONS				
SYMMETRY $\frac{\phi}{2}$				
RADI				
DECIMALS		 APPROVED		
.X				
.XX				
.XXX		RELEASE DATE		
.XXXX		N/A		
ANGLES		ORIGINAL RELEASE DATE		
		N/A		
B/F	N/A	P/C	853	

GLENAIR, INC.				
1211 AIR WAY, GLENDALE, CALIFORNIA 91201				
TITLE JACK, BOARD, PIN RIGHT ANGLE, BAYONET VERSALINK BRIDGE				
CODE IDENT. NO.	SIZE	DWG NO	REV	
06324	B	853-067	2	
SCALE: N/A		WEIGHT: N/A	SHEET 1 OF 1	