



GT-19-230

VersaLink Micro-D

High Speed Characterization Report for Differential Applications



Revision History

Rev	Date	Approved	Description
A	2/7/2023	L. Blackwell / B. Samowitz	Initial Release
B	1/25/2024	L. Blackwell	Added USP results per DCN100150



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1. Introduction

This document contains results from testing that was performed to evaluate the high-frequency electrical performance of the Glenair VersaLink Micro-D in differential signaling applications. This report outlines frequency domain performance metrics such as insertion loss (IL) and return loss (RL) as well as time-domain performance metrics including impedance and eye diagrams.

2. Product Overview

The Glenair VersaLink delivers outstanding impedance matching and crosstalk isolation at both the cable-to-connector interface, as well as between connector and board. VersaLink is a highly engineered differential Twinax contact module that may be packaged in a wide range of both circular and rectangular connector formats such as the MIL-DTL-83513 Micro-D. This high-density package solution provides mating reliability, ruggedness, signal integrity, and deployment simplicity.

3. Test Setup

This section details the test assemblies, test PCBs and equipment used to perform the high-speed characterization. All measurements were taken using a Tektronix DSA8300 Digital Serial Analyzer and a Keysight E5071C network analyzer which were connected to SMA-launch test fixture PCBs designed specifically for this testing.

3.1. Test Fixtures

3.1.1. Test PCBs

Test fixture PCB sets utilizing edge-launch SMA connectors were designed for the high-speed tests. Each set consisted of a VersaLink Micro-D to SMA board and a calibration board. Calibration board performance data is included in Appendix A. One test set used straight VersaLink Micro-D PCB-mount connectors, part numbers GVLM2L-4-0PBSPN-.080 and GVLM2L-4-0SBSPN-.080. The other set used right-angle VersaLink Micro-D PCB-mount connectors, part numbers GVLM2L-4-0PBRLT-.080 and GVLM2L-4-0SBRPT-.080. Photographs of the test boards are seen in the following two figures.

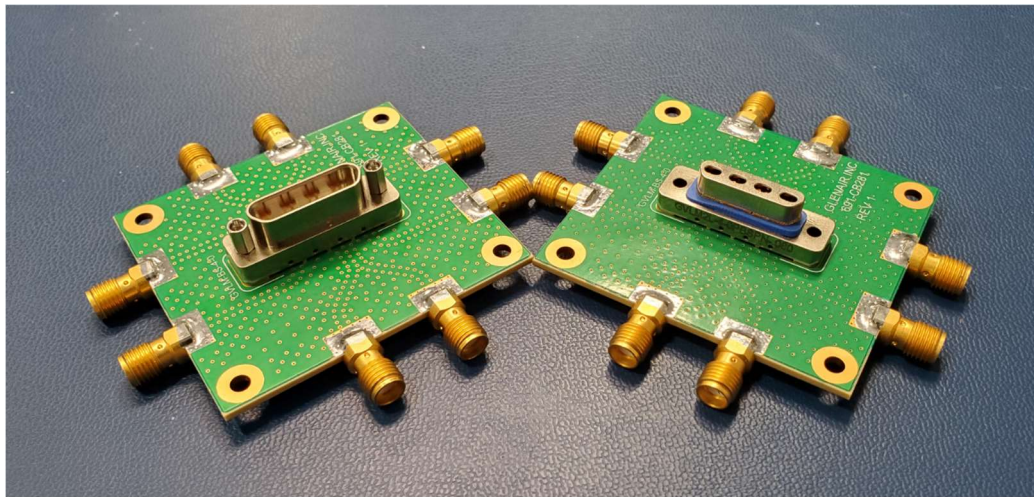


Figure 1. VersaLink Micro-D Straight Test PCB

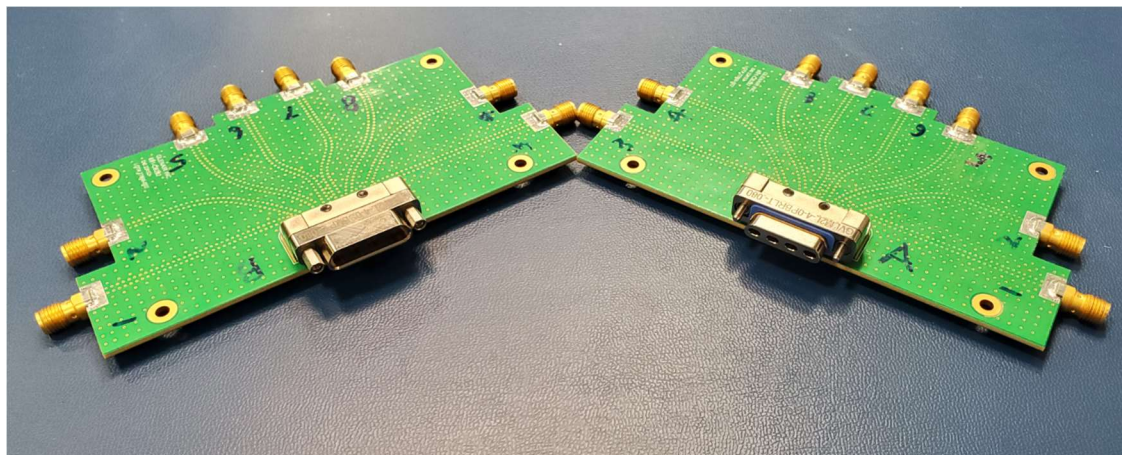


Figure 2. VersaLink Micro-D Right-Angle Test PCB

The board sets were manufactured as a single panel and separated into individual test boards to give consistent signal characteristics.

3.1.2. Test Cable Assemblies

In addition to the test PCBs, an experimental VersaLink Micro-D cable assembly was tested. The assembly is presented in Figure 3.

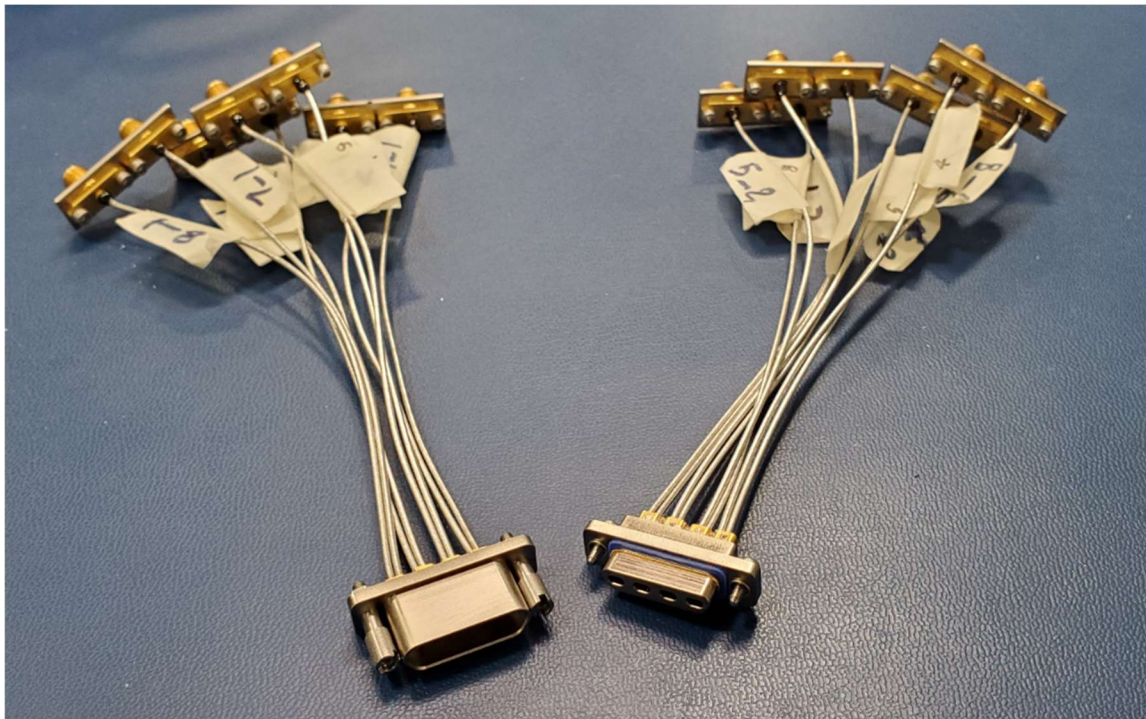


Figure 3. VersaLink Micro-D Test Cable Assembly

3.1.3. Sav-Con Test Assembly

The VersaLink Micro-D Sav-Con Test Assembly consisted of a GVLM-USP1 connector inserted between the two segments of the VersaLink Micro-D Test Cable Assembly in the above section. The assembly is show below in Figure 4.

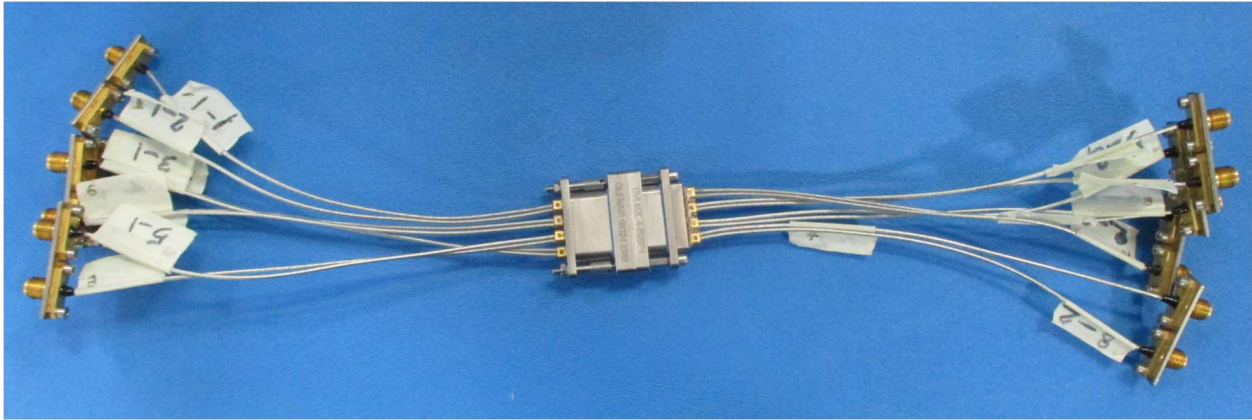


Figure 4. VersaLink Micro-D Sav-Con Test Assembly

4. Straight VersaLink Micro-D Performance

This section includes both frequency and time domain results. Test fixture PCB and test cabling loss have been de-embedded to show the performance of the assembly only.

4.1. Frequency Domain Analysis

4.1.1. Straight VersaLink Micro-D Insertion Loss

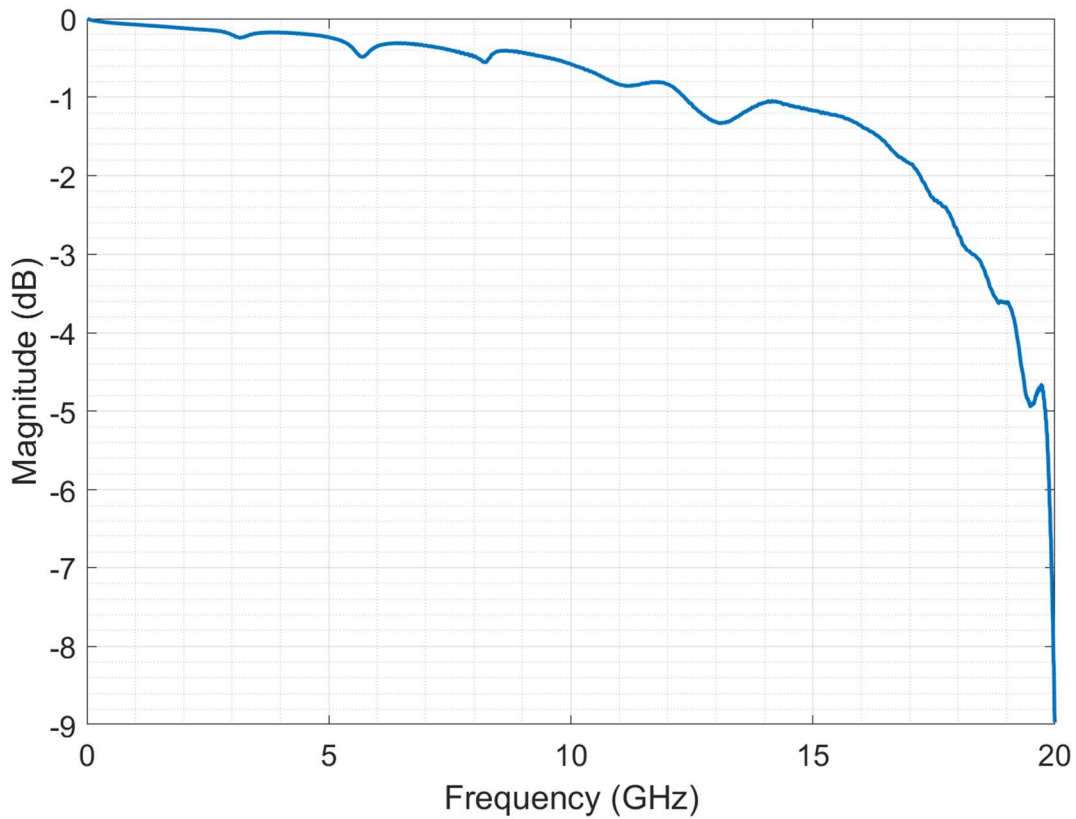


Figure 5. Straight VersaLink Micro-D Insertion Loss

4.1.2. Straight VersaLink Micro-D Return Loss

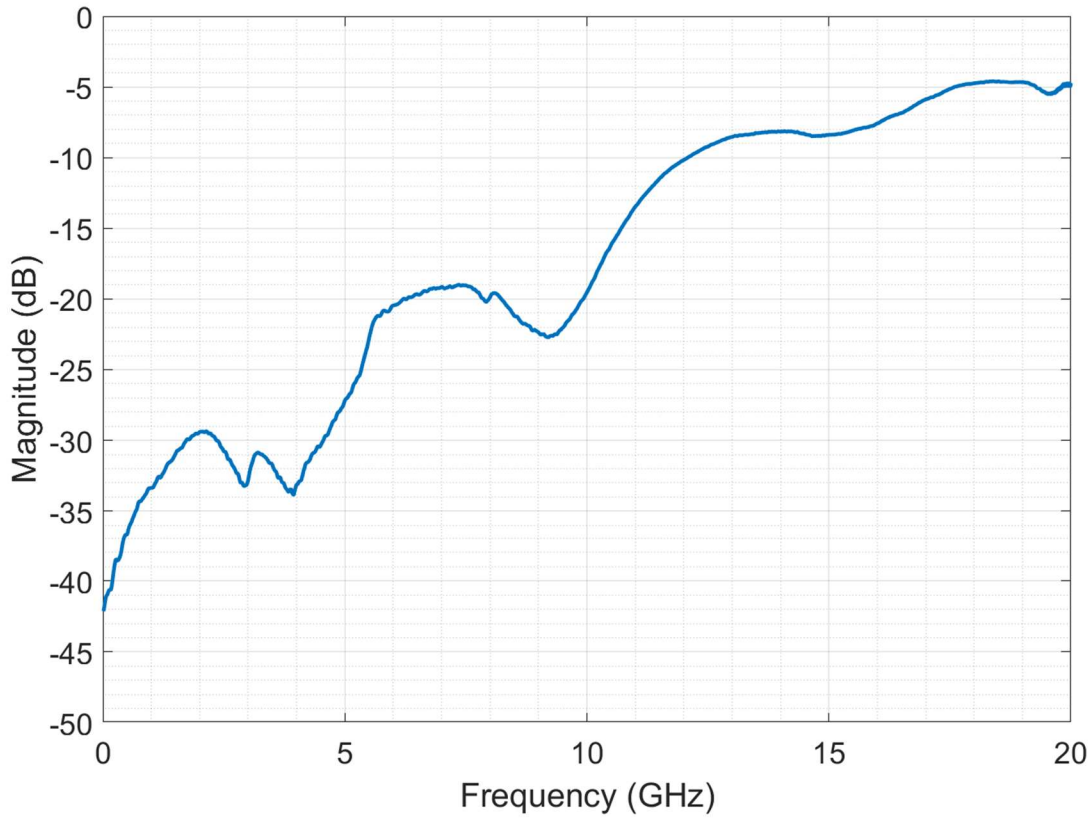


Figure 6. Straight VersaLink Micro-D Return Loss

4.1.3. Straight VersaLink Micro-D VSWR

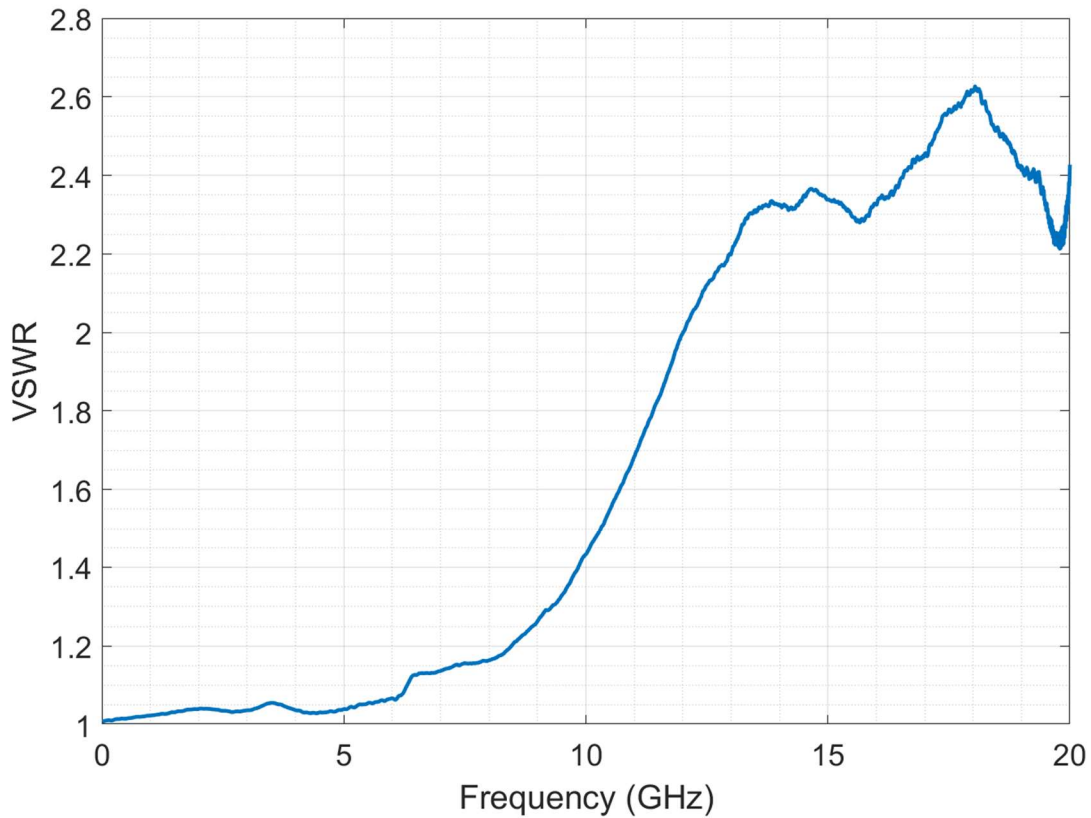


Figure 7. Straight VersaLink Micro-D VSWR

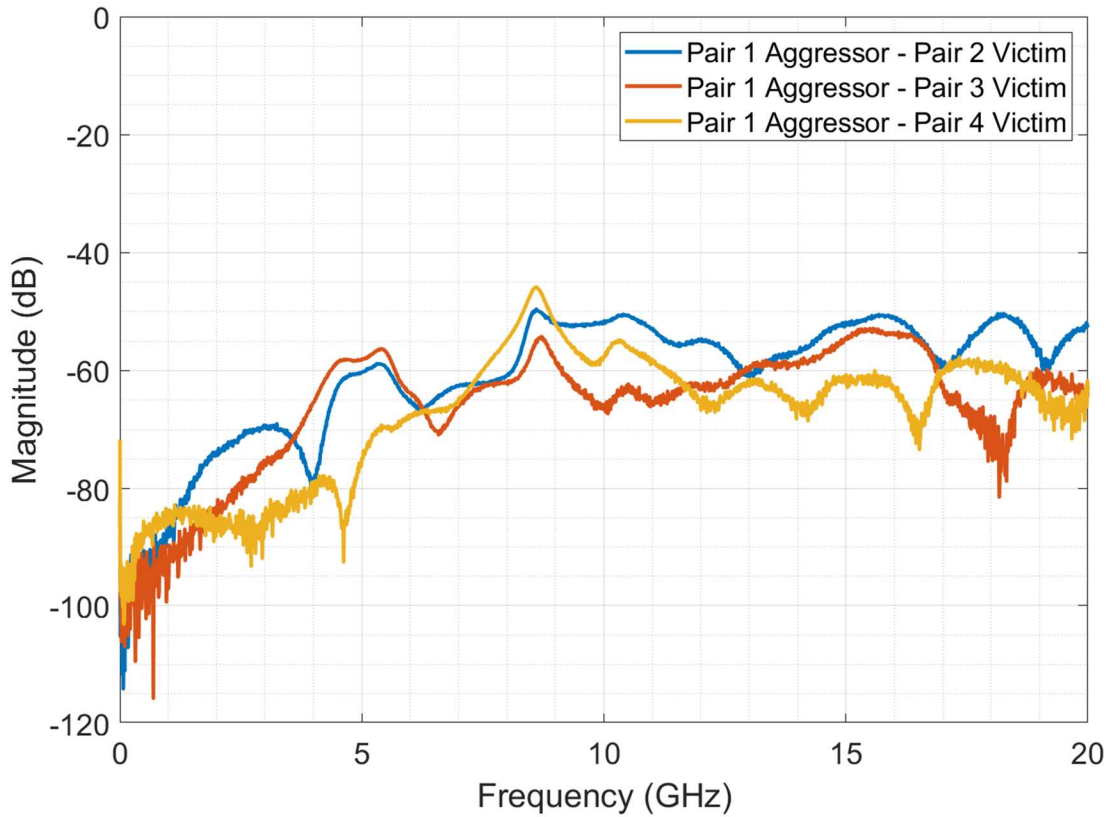


Figure 8. Straight VersaLink NEXT

4.2. Straight VersaLink Micro-D Time Domain Analysis

4.2.1. Straight VersaLink Micro-D TDR

Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW (GHz)
25	14
35	10

50	7
100	3.5

Table 1. Bandwidth to Rise Time Relationship

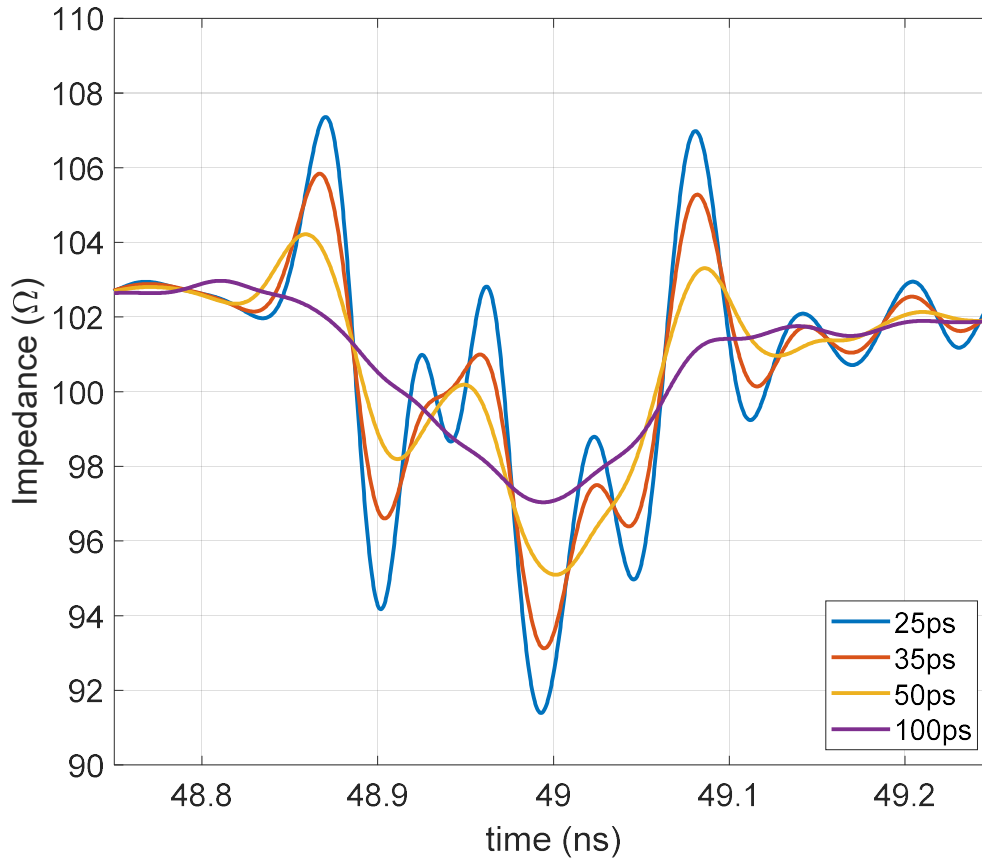


Figure 9. TDR – Straight VersaLink Micro-D

4.2.2. Straight VersaLink Micro-D Eye Diagram

The S-parameter data for Pair 1 obtained from the Keysight N5227B PNA measurements was used to generate a statistical eye diagram for a bit rate of 28Gbps and is presented in Figure 10

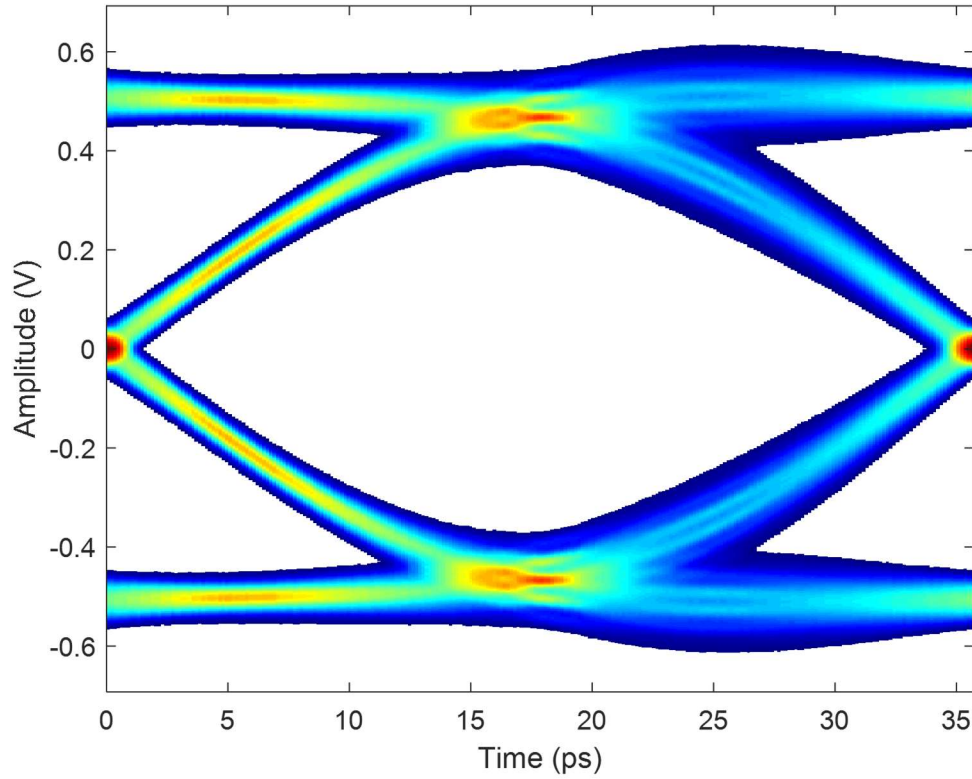


Figure 10. Eye diagram of Straight VersaLink Micro-D at 28Gbps

5. Right-Angle VersaLink Micro-D Performance Summary

This section includes both frequency and time domain results. Test fixture PCB and test cabling loss have been de-embedded to show the performance of the assembly only.

5.1. Frequency Domain Analysis

5.1.1. Right-Angle VersaLink Micro-D Insertion Loss

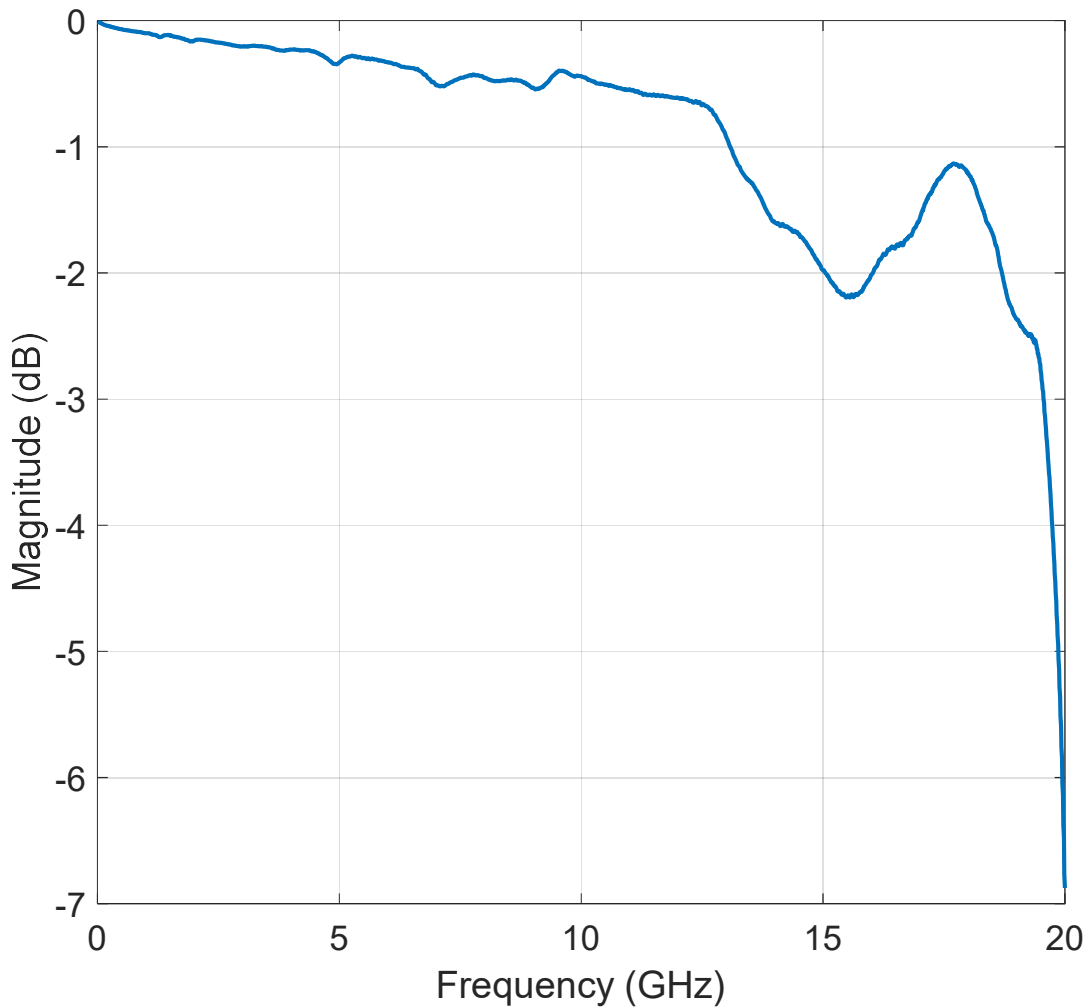


Figure 11. Right-Angle VersaLink Micro-D Insertion Loss

5.1.2. Right-Angle VersaLink Micro-D Return Loss

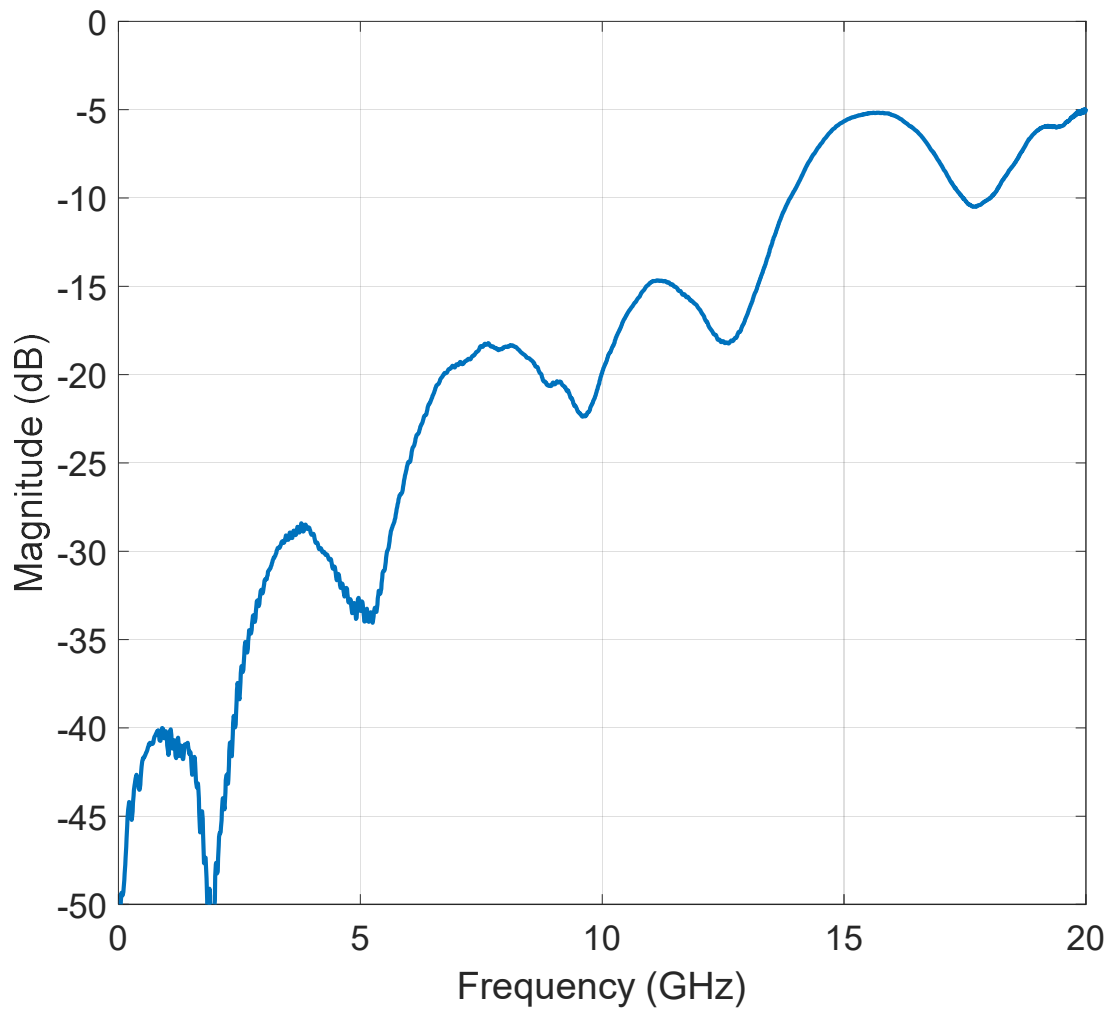


Figure 12. Right-Angle VersaLink Micro-D Return Loss

5.1.3. Right-Angle VersaLink Micro-D VSWR

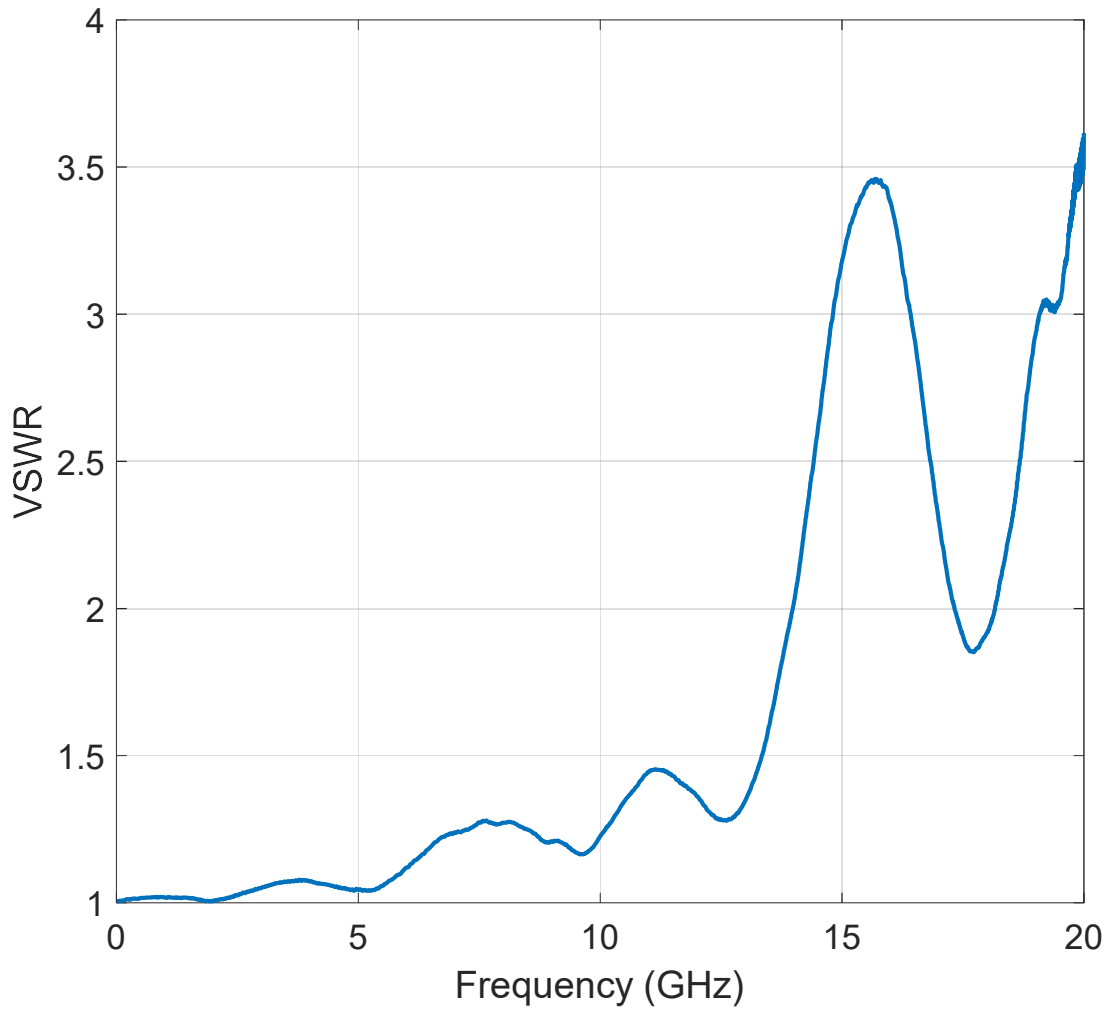


Figure 13. Right-Angle VersaLink Micro-D VSWR

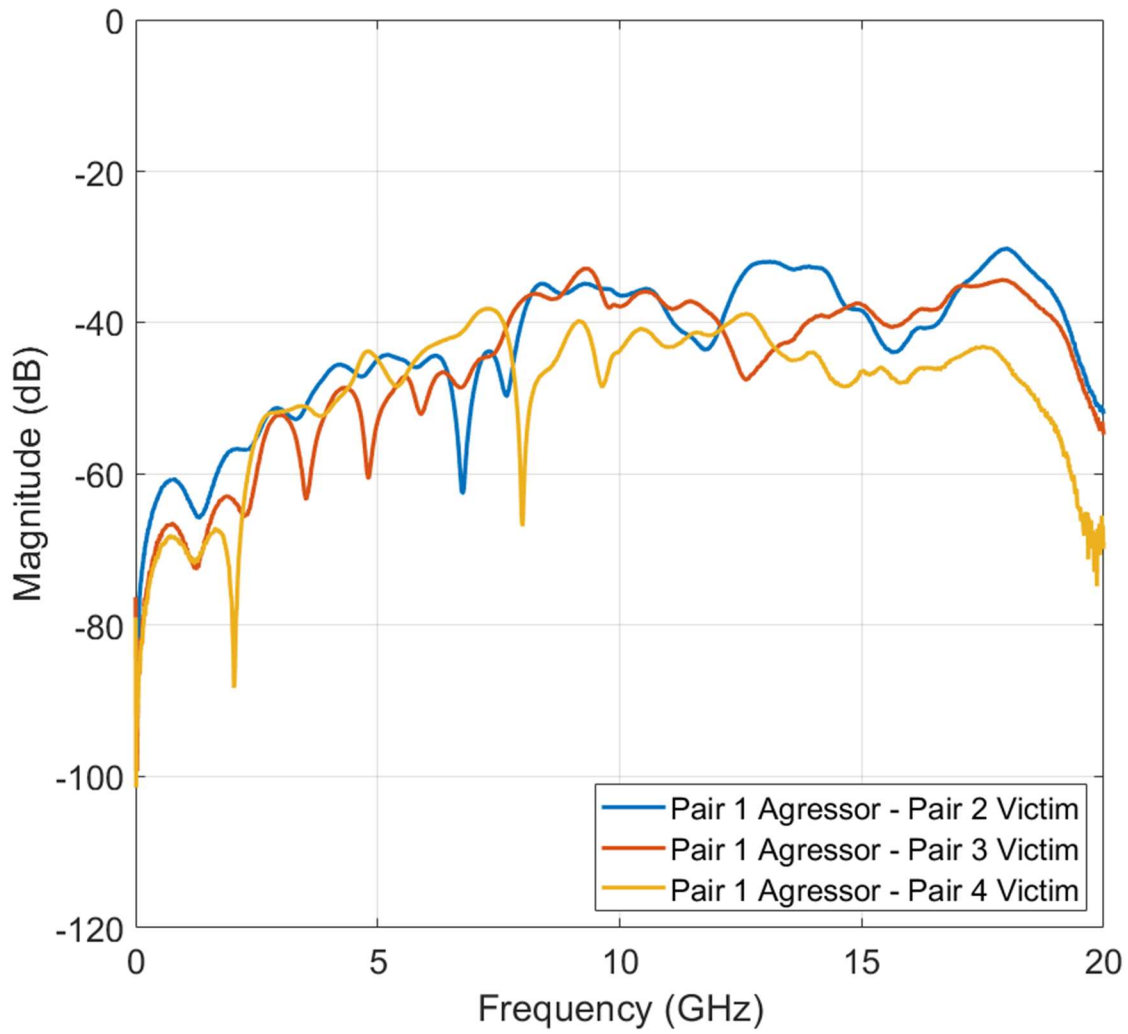


Figure 14. Right-Angle VersaLink NEXT

5.2. Time Domain Analysis

5.2.1. Right-Angle VersaLink Micro-D TDR

Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW (GHz)
25	14
35	10
50	7
100	3.5

Table 2. Bandwidth to Rise Time Relationship

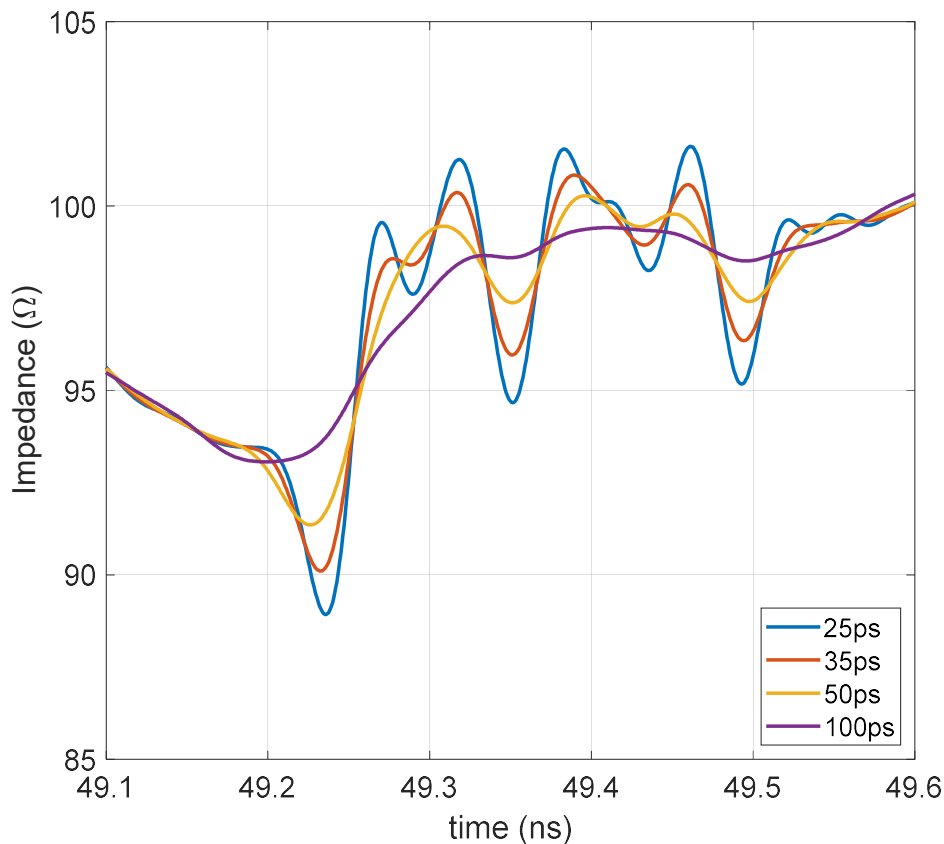


Figure 15. TDR – Right-Angle VersaLink Micro-D

5.2.2. Right-Angle VersaLink Micro-D Eye Diagrams

The S-parameter data for Pair 1 obtained from the Keysight N5227B PNA measurements was used to generate a statistical eye diagram for a bit rate of 28Gbps and is presented in Figure 16.

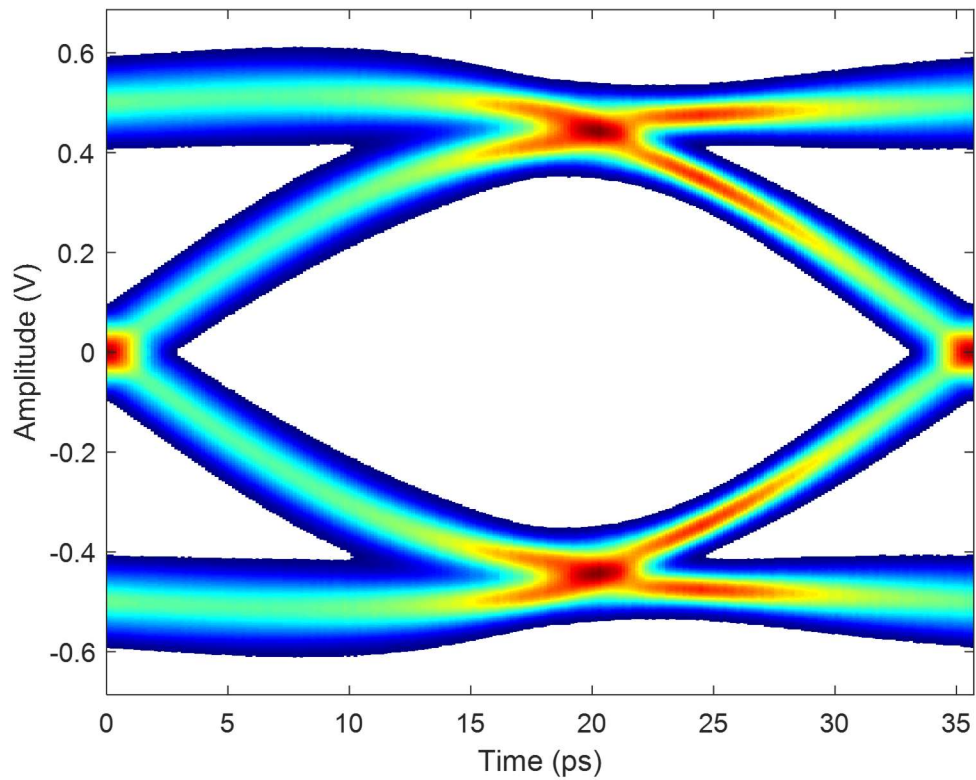


Figure 16. Eye diagram of Right-Angle VersaLink Micro-D at 28Gbps

6. VersaLink Micro-D Cable Assembly Performance

6.1. VersaLink Micro-D Cable Assembly Frequency Domain Analysis

6.1.1. VersaLink Micro-D Cable Assembly Insertion Loss

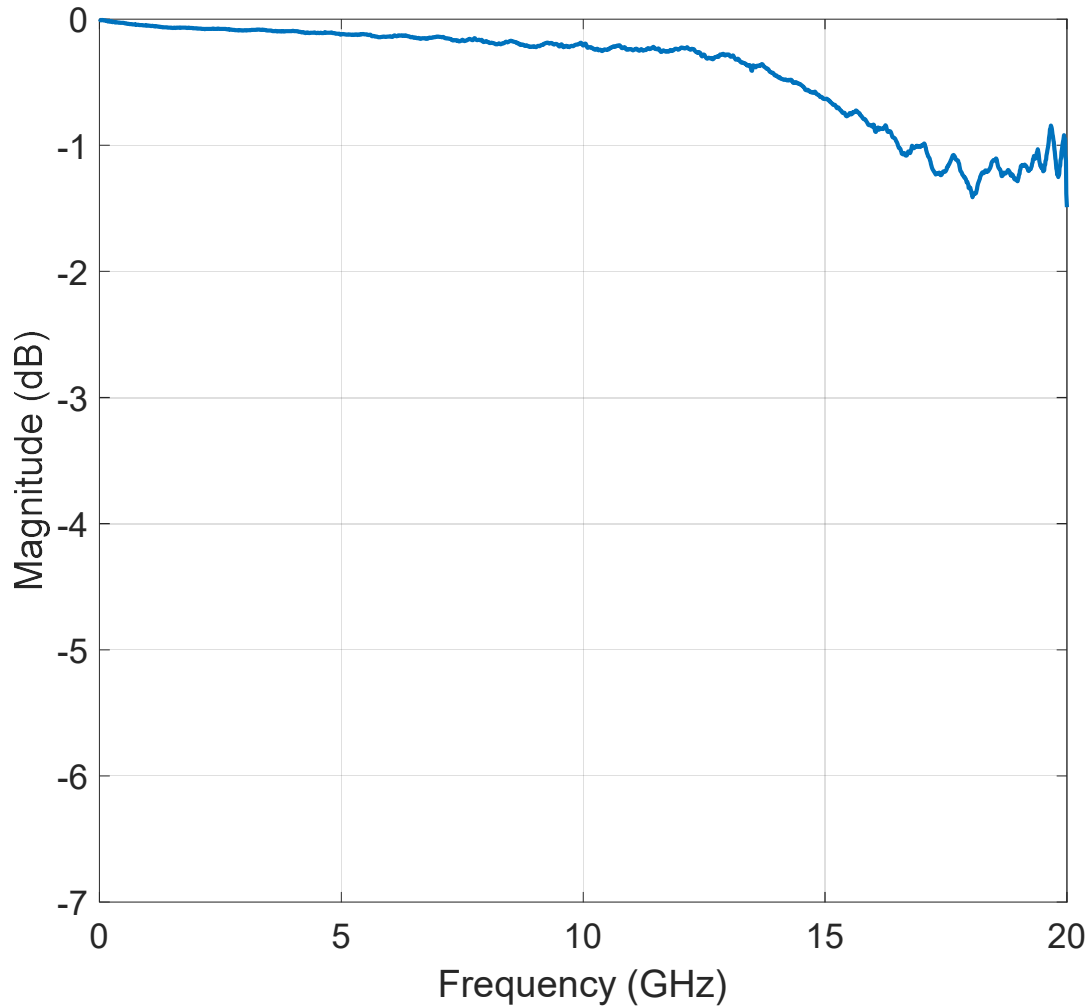


Figure 17. VersaLink Micro-D Cable Assembly Insertion Loss

6.1.2. VersaLink Micro-D Cable Assembly Return Loss

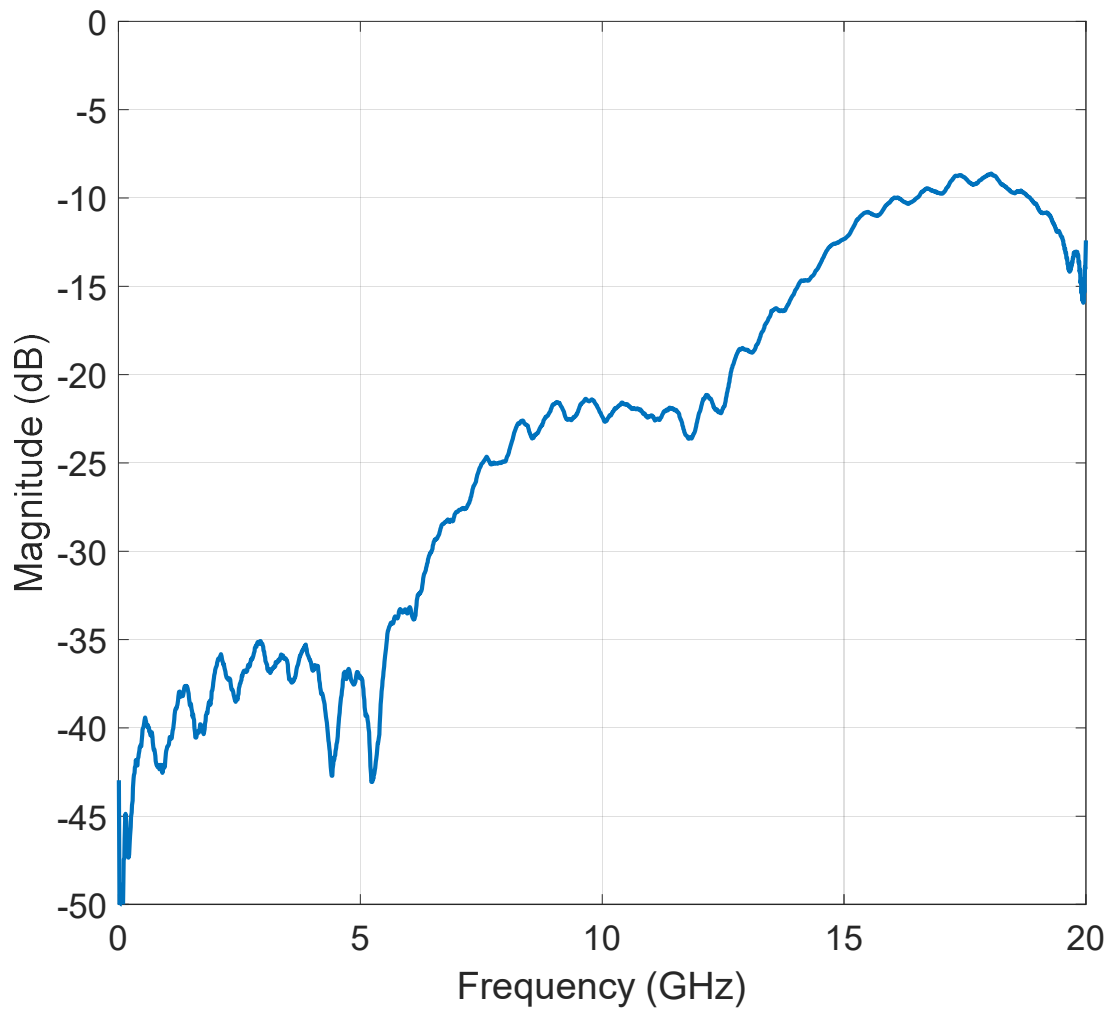


Figure 18. VersaLink Micro-D Cable Assembly Return Loss

6.1.3. VersaLink Micro-D Cable Assembly VSWR

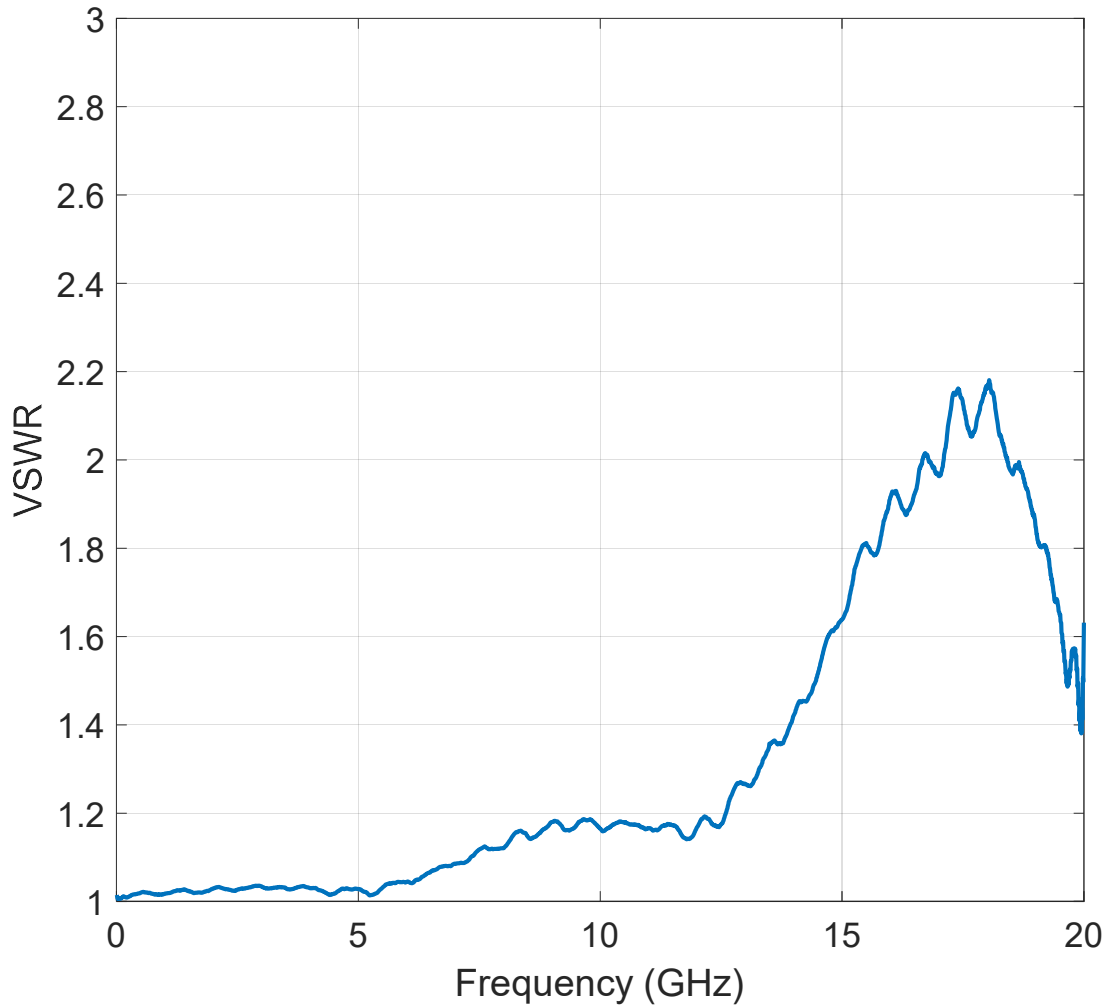


Figure 19. VersaLink Micro-D Cable Assembly VSWR

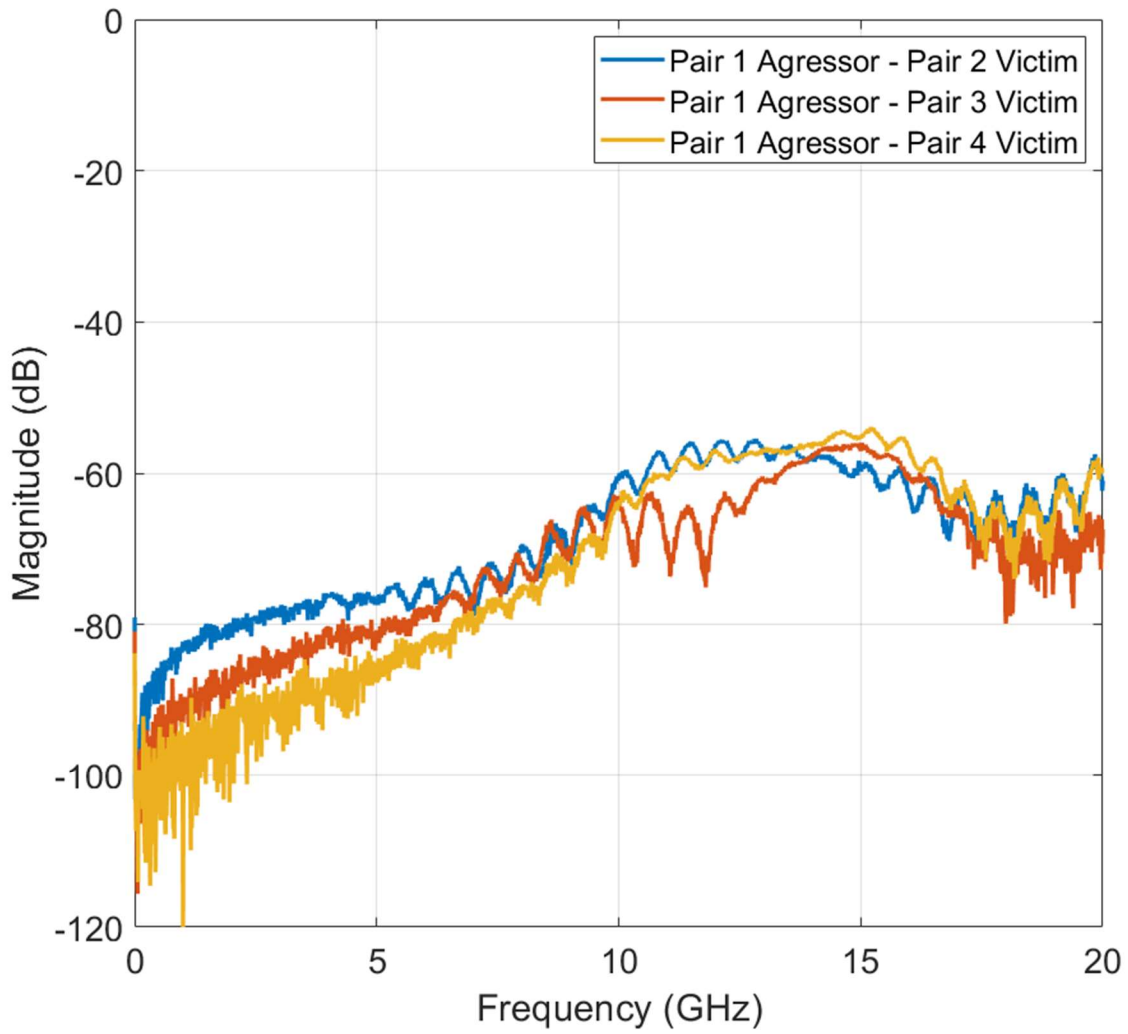


Figure 20. VersaLink Micro-D Cable Assembly NEXT

6.2.VersaLink Micro-D Cable Assembly Time Domain Analysis

6.2.1. VersaLink Micro-D Cable Assembly TDR

Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
25	14
35	10
50	7
100	3.5

Table 3. Bandwidth to Rise Time Relationship

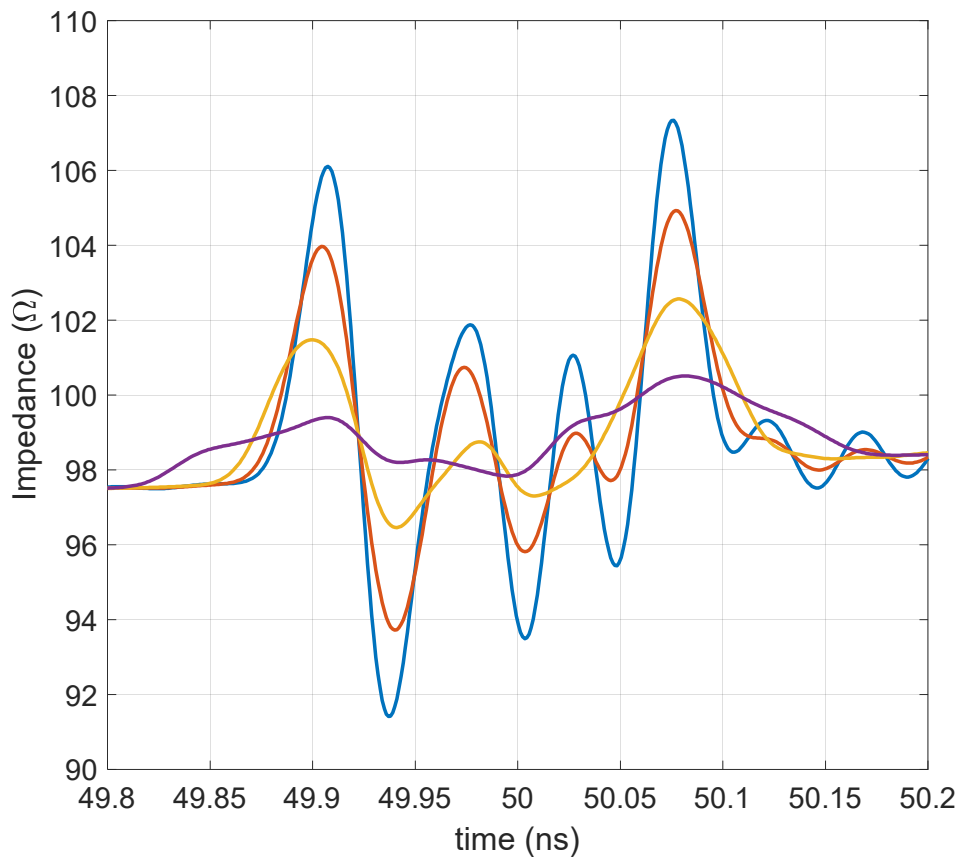


Figure 21. VersaLink Micro-D Cable Assembly TDR

6.2.2. VersaLink Micro-D Cable Assembly Eye Diagram

The S-parameter data for Pair 1 obtained from the Keysight N5227B PNA measurements was used to generate a statistical eye diagram for a bit rate of 28Gbps and is presented in Figure 22.

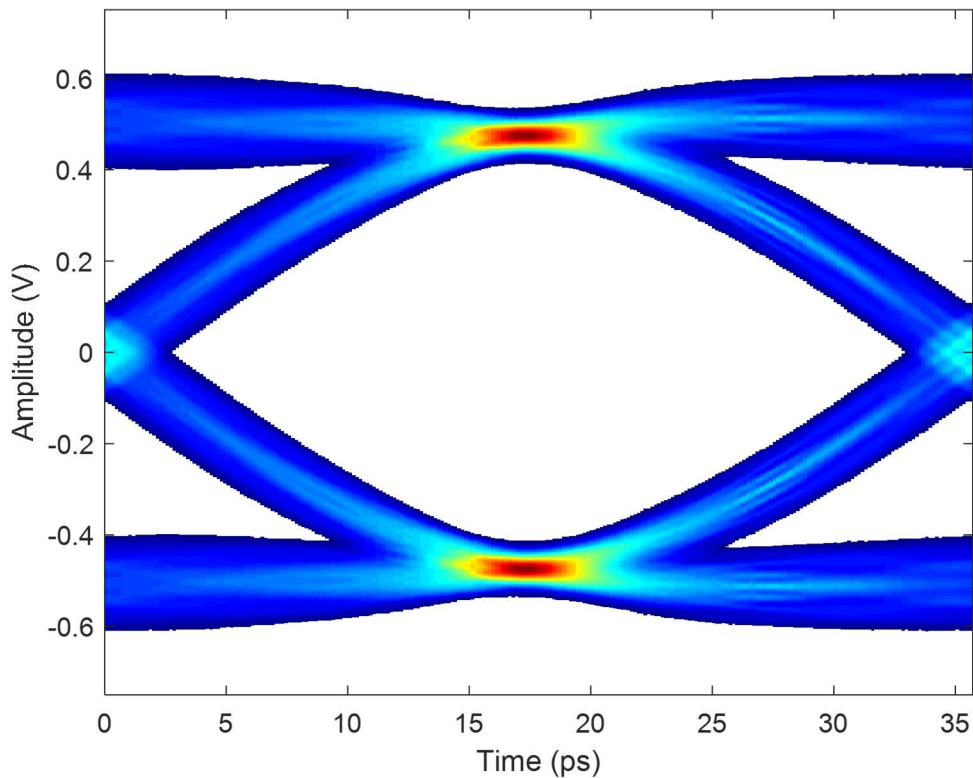


Figure 22. Eye diagram of VersaLink Micro-D Cable Assembly at 28Gbps

7. VersaLink Micro-D Sav-Con Test Assembly Performance

7.1. VersaLink Micro-D Sav-Con Assembly Frequency Domain Analysis

7.1.1. VersaLink Micro-D Sav-Con Assembly Insertion Loss

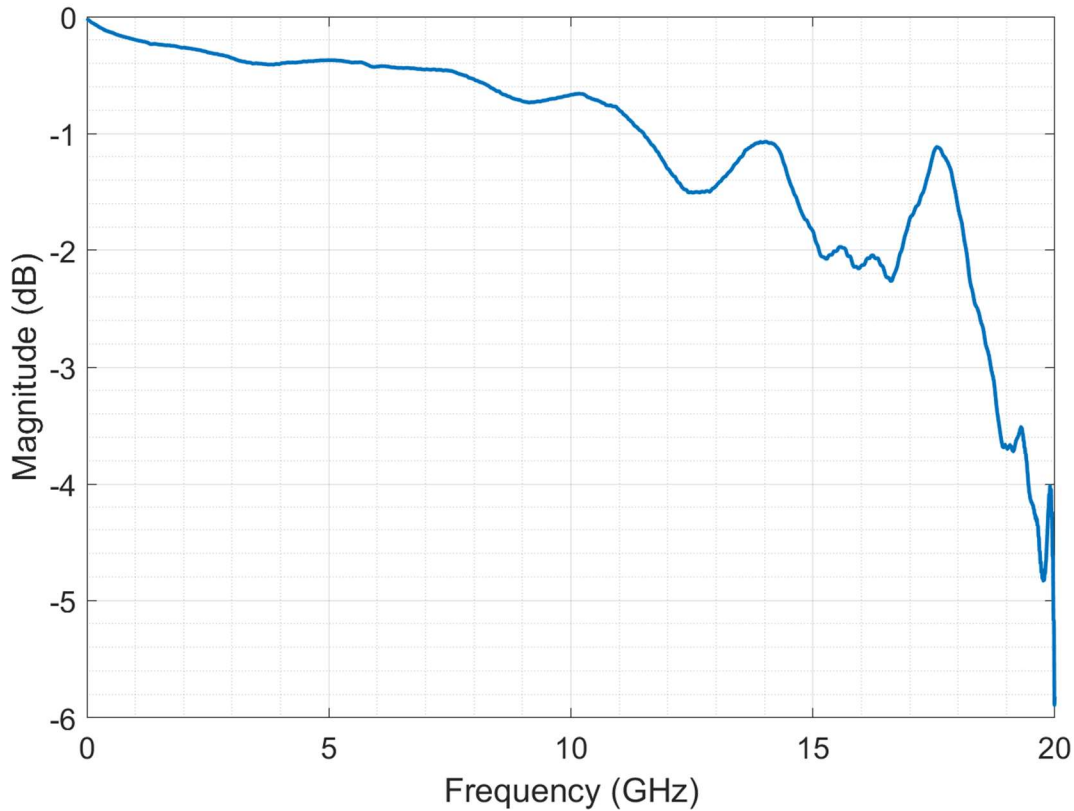


Figure 23. VersaLink Micro-D Sav-Con Assembly Insertion Loss

7.1.2. VersaLink Micro-D Sav-Con Assembly Return Loss

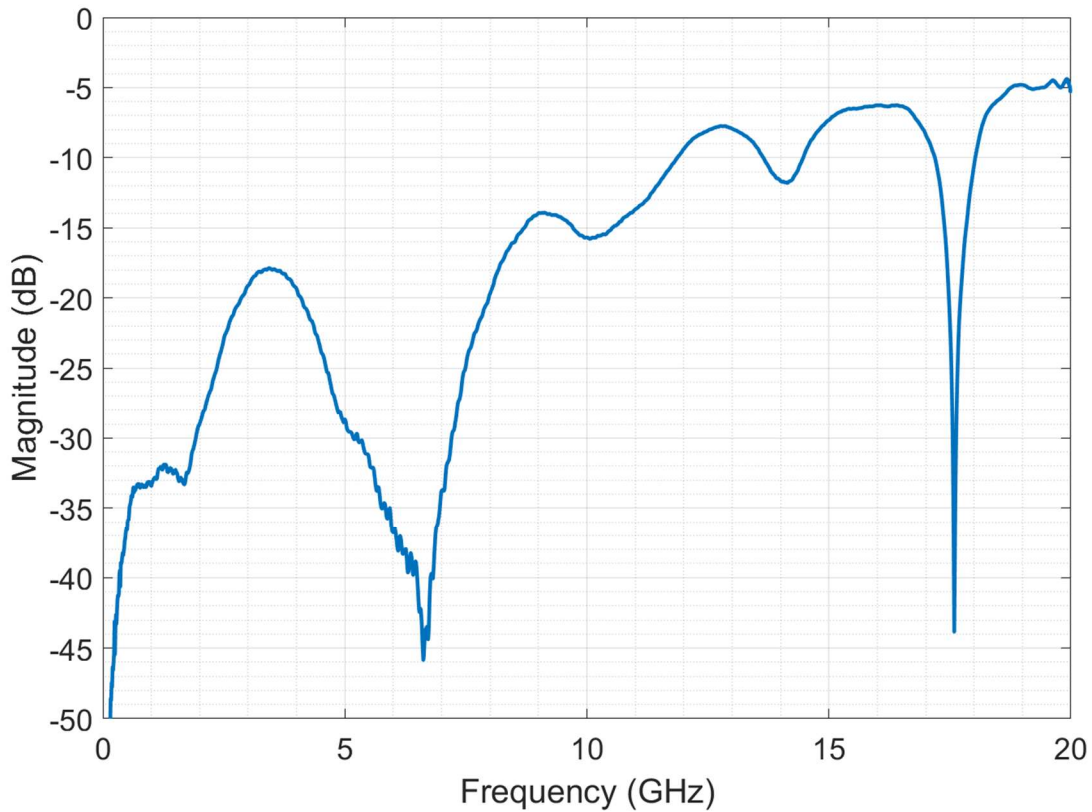


Figure 24. VersaLink Micro-D Sav-Con Assembly Return Loss

7.1.3. VersaLink Micro-D Sav-Con Assembly VSWR

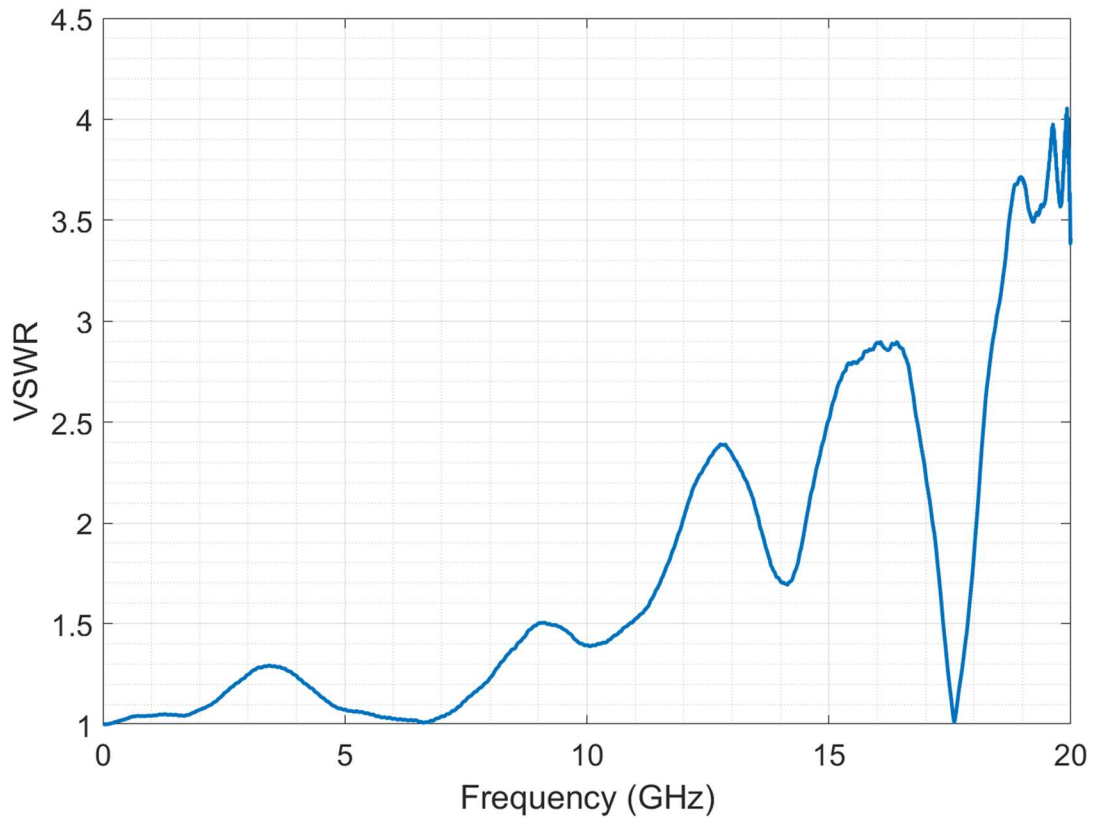


Figure 25. VersaLink Micro-D Sav-Con Assembly VSWR

7.1.4. VersaLink Micro-D Sav-Con Assembly NEXT

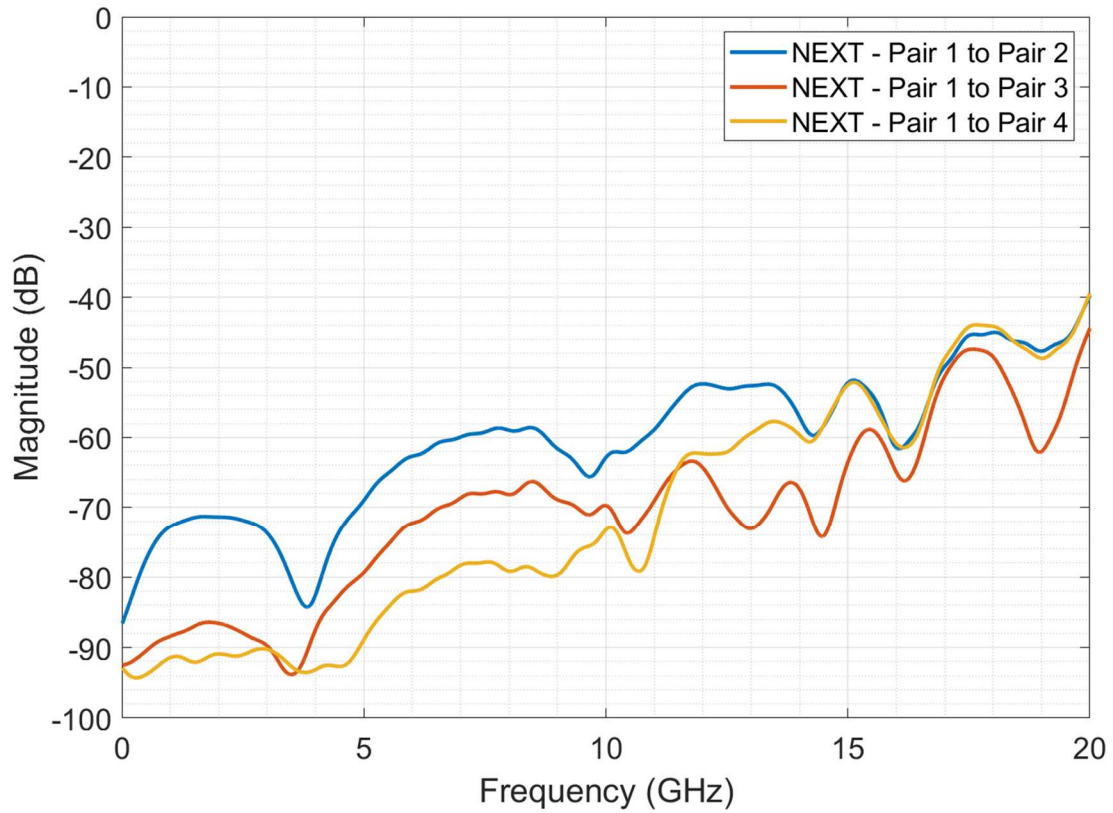


Figure 26. VersaLink Micro-D Sav-Con Assembly NEXT

7.1.5. VersaLink Micro-D Sav-Con Assembly FEXT

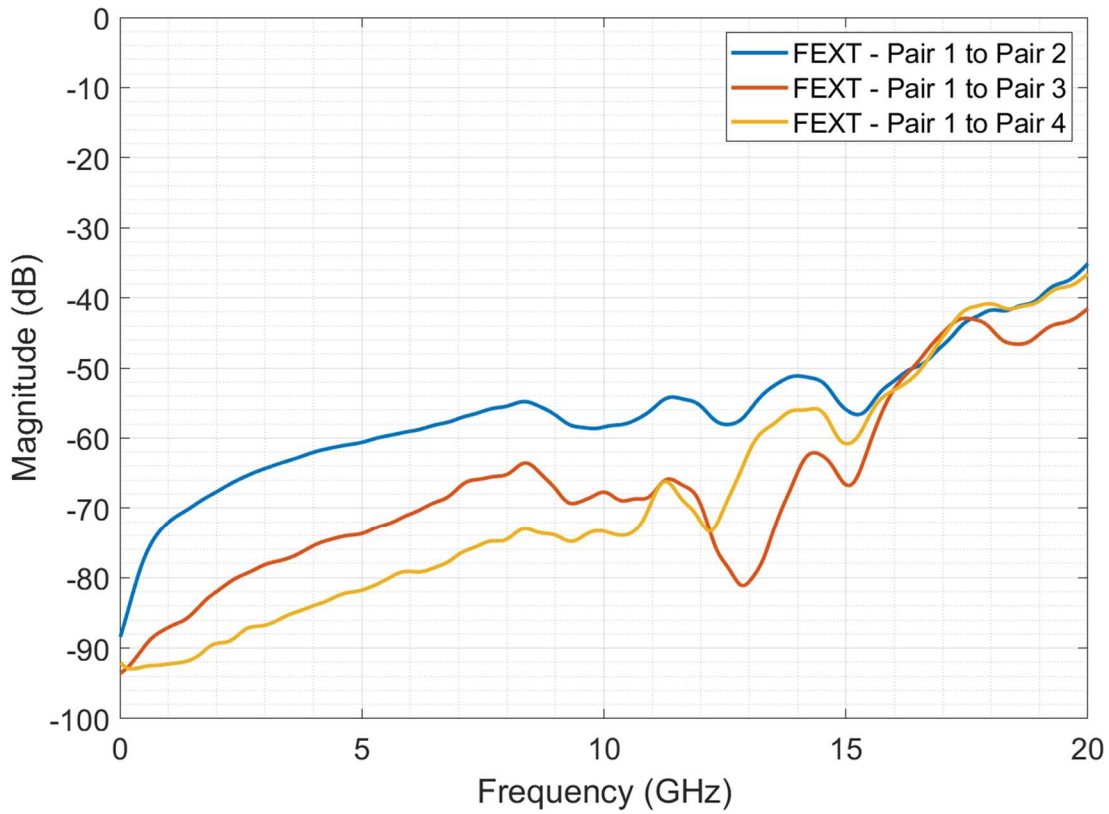


Figure 27. VersaLink Micro-D Sav-Con Assembly FEXT

7.2. VersaLink Micro-D Sav-Con Test Assembly Time Domain Analysis

7.2.1. VersaLink Micro-D Sav-Con Assembly TDR

Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW (GHz)
25	14
50	7
100	3.5

Table 4. Bandwidth to Rise Time Relationship

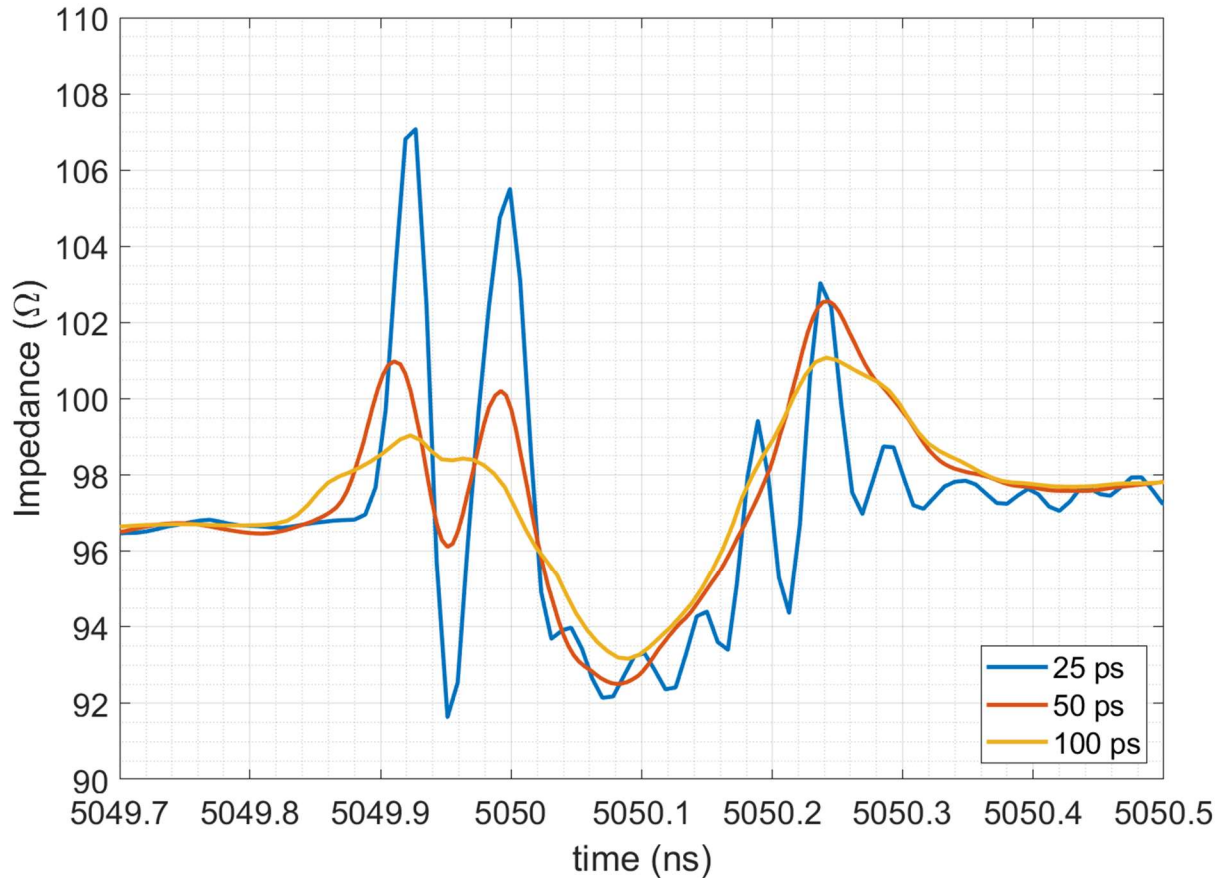


Figure 28. VersaLink Micro-D Sav-Con Assembly TDR

7.2.2. VersaLink Micro-D Sav-Con Assembly Eye Diagram

The S-parameter data for Pair 1 obtained from the Keysight N5227B PNA measurements was used to generate a statistical eye diagram for a bit rate of 28Gbps and is presented in Figure 29.

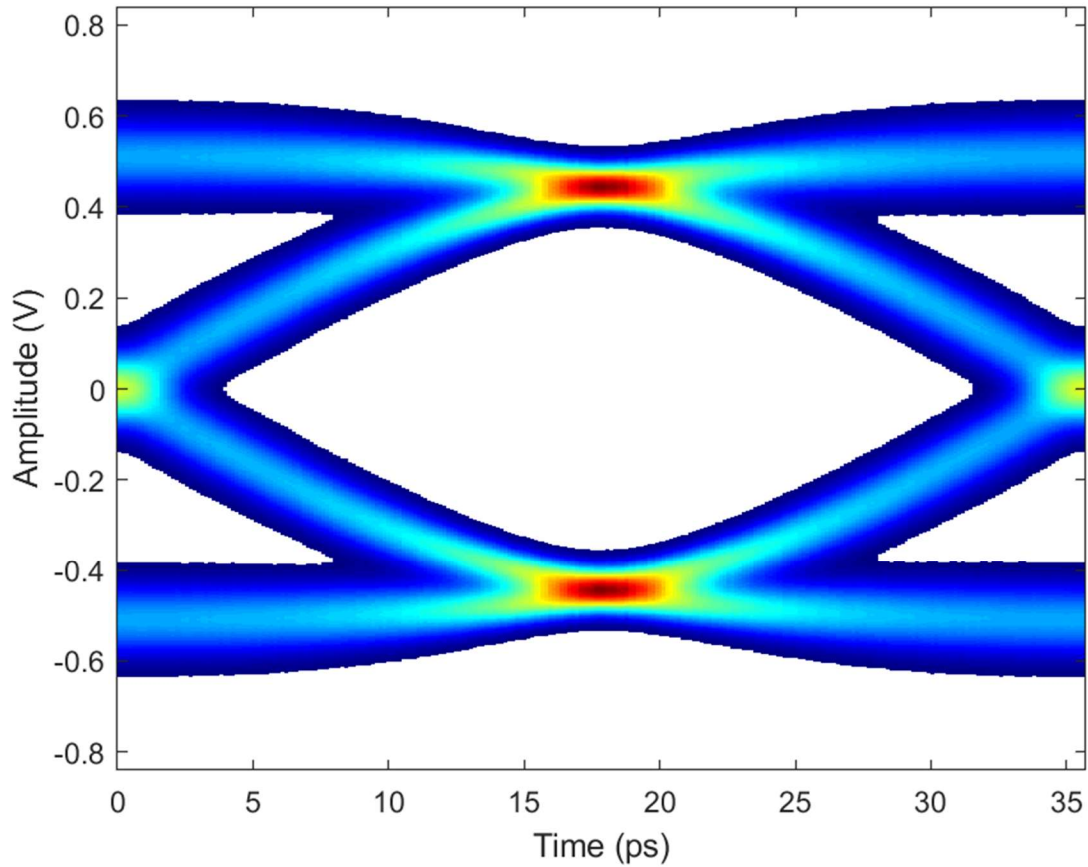


Figure 29. Eye diagram of VersaLink Micro-D Sav-Con Assembly at 28Gbps

Appendix A. 2x-Thru Fixture Performance

This section includes frequency domain results of the 2x-thru PCBs and cable assembly used to extract the VersaLink Micro-D electrical characteristics from the overall measured DUT/fixtures data.

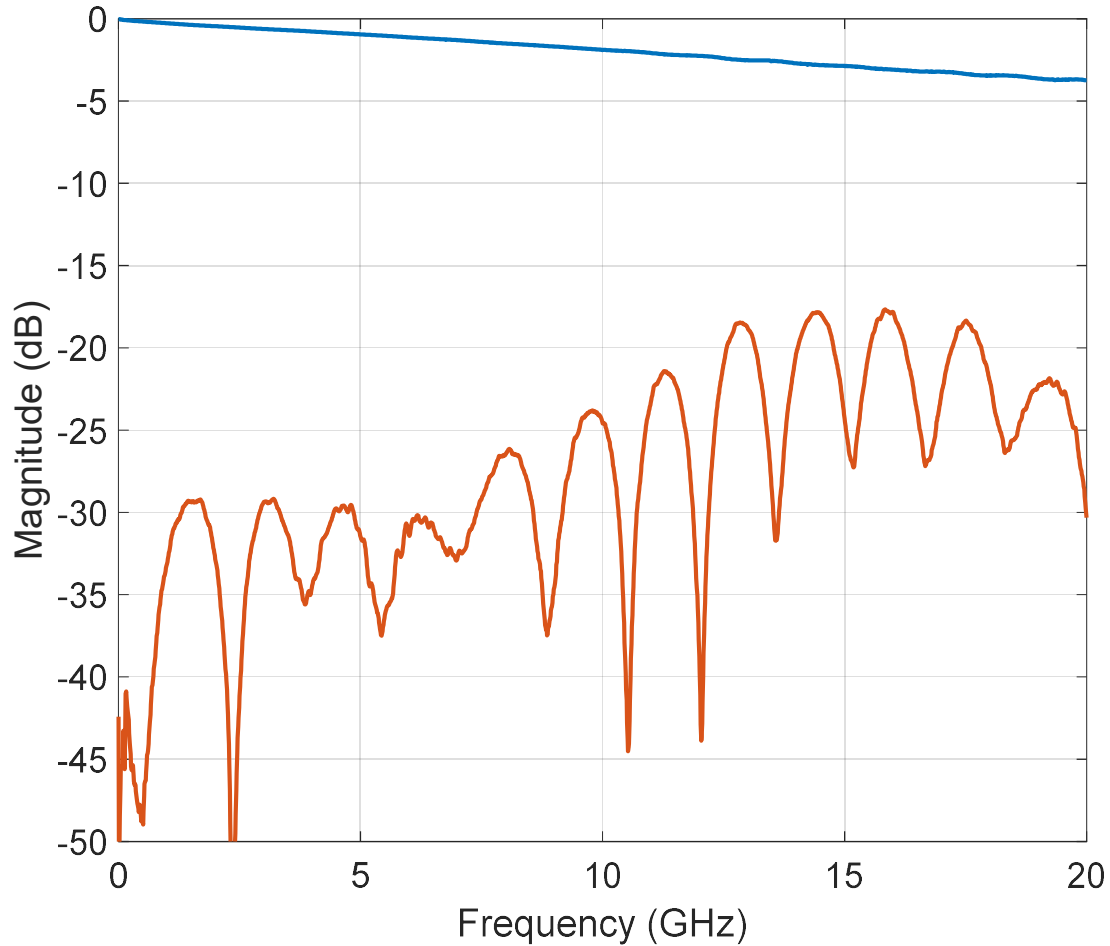


Figure 30. Straight VersaLink Micro-D 2x-Thru PCB Response

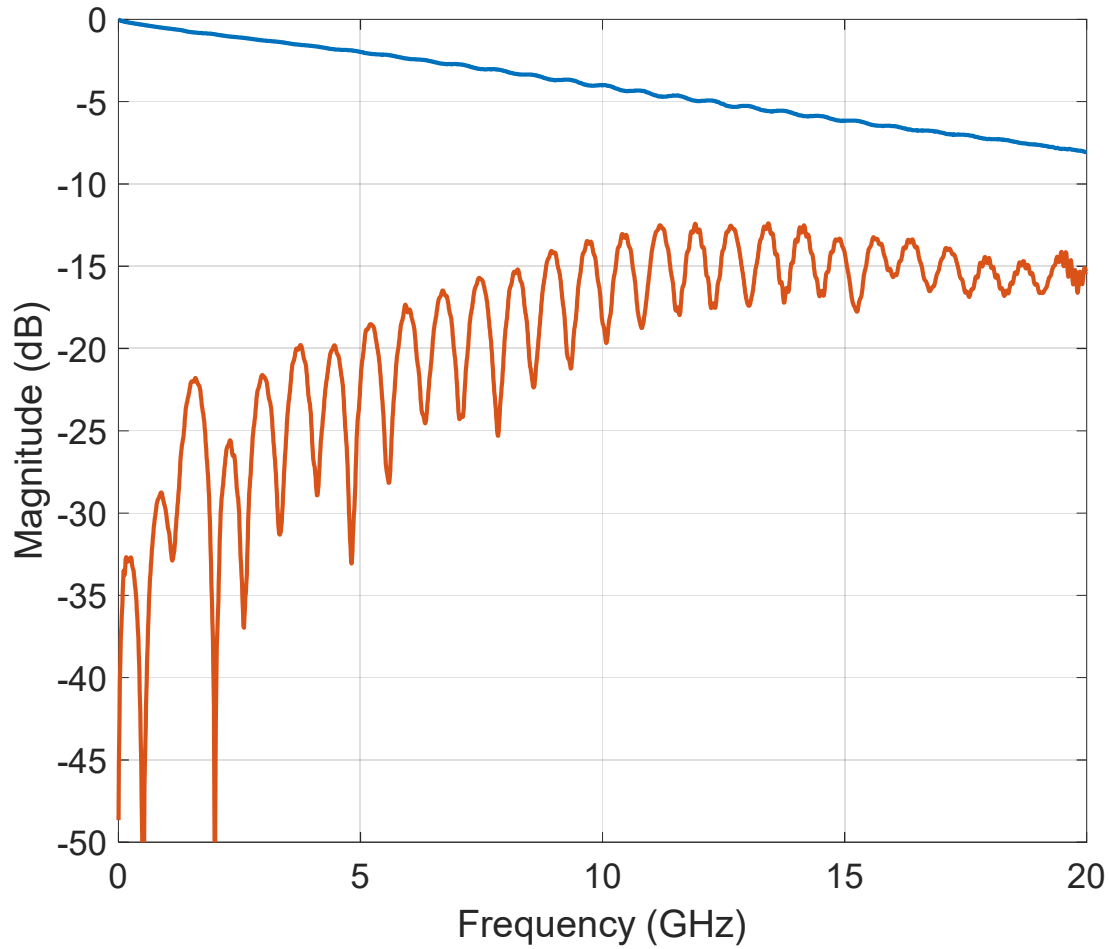


Figure 31. Right Angle VersaLink Micro-D 2x-Thru PCB Response

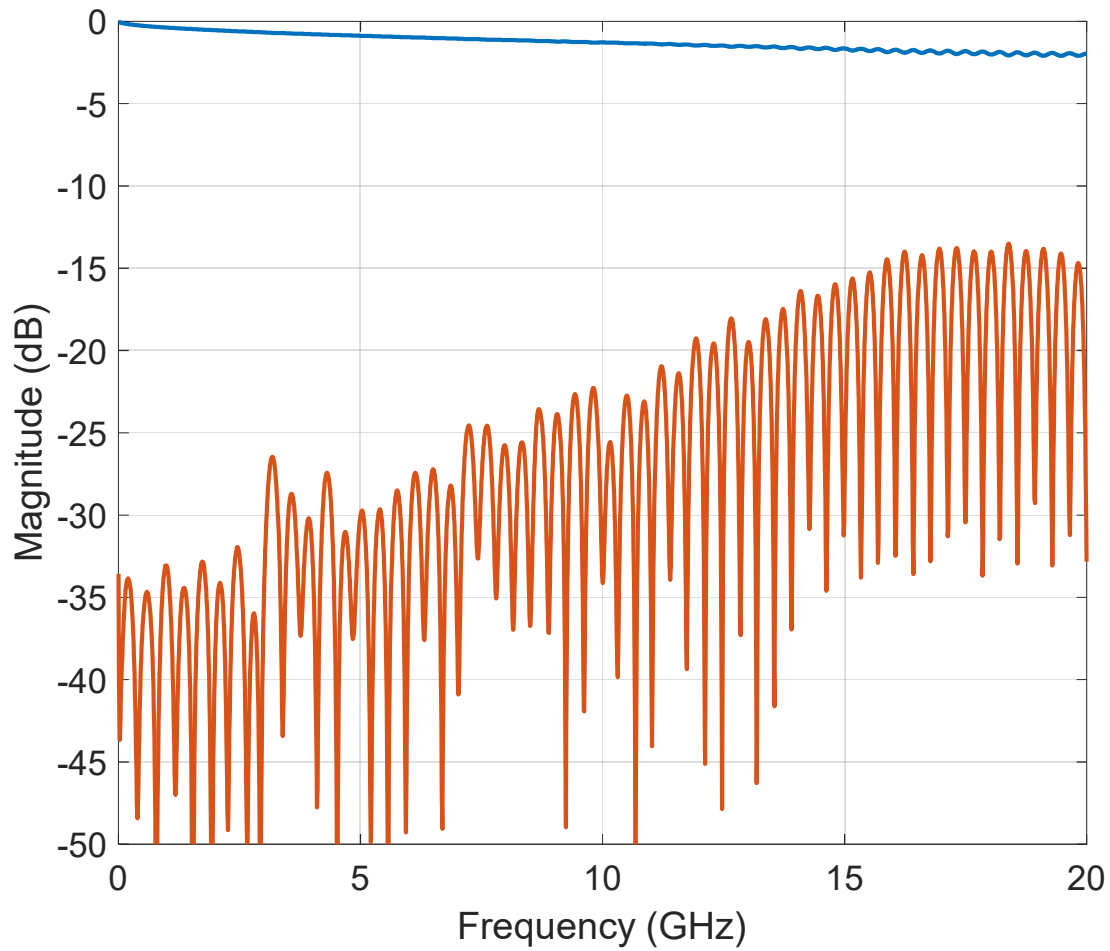


Figure 32. VersaLink Micro-D Cable Assembly 2x-Thru Response