



GT-22-112

Glenair High-Speed Micro-D High Speed Characterization Report for Ethernet Applications



Revision History

Rev	Date	Approved	Description
1	8/14/2024	L. Blackwell	Initial Release
2	6/25/2025	L. Blackwell	Added Feedthru and Unisaver data
3	10/6/2025	L. Blackwell	Added link to S-parameter app note



Table of Contents

1. Introduction	7
2. Product Overview	7
3. Test Setup	7
3.1. Test Fixtures	8
3.1.1. Test Assemblies	8
3.2. Test Pairs	10
4. Performance of Straight PC Tail GHSM-BSS Mated Pair	11
4.1. Frequency Domain Analysis	11
4.1.1. Insertion Loss – GHSM-BSS Mated Pair	11
4.1.2. Return Loss - GHSM-BSS Mated Pair	12
4.1.3. NEXT - GHSM-BSS Mated Pair	13
4.1.4. FEXT - GHSM-BSS Mated Pair	14
4.2. Time Domain Analysis - GHSM-BSS Mated Pair.....	15
5. Performance of Right-Angle PC Tail GHSM-HBR Mated Pair.....	16
5.1. Frequency Domain Analysis	16
5.1.1. Insertion Loss – GHSM-HBR Mated Pair	16
5.1.2. Return Loss – GHSM-HBR Mated Pair	17
5.1.3. NEXT- GHSM-HBR Mated Pair.....	18
5.1.4. FEXT – GHSM-HBR Mated Pair	19
5.2. Time Domain Analysis – GHSM-HBR Mated Pair.....	20
6. Performance of Wired Connector GHS7M-1005-6 Mated With Straight PC Tail GHSM-BSS 21	
6.1. Frequency Domain Analysis	21
6.1.1. Insertion Loss – GHS7M-1005-6 Mated With GHSM-BSS	21
6.1.2. Return Loss - GHS7M-1005-6 Mated With GHSM-BSS	22
6.1.3. NEXT – GHS7M-1005-6 Mated With GHSM-BSS	23
6.1.4. FEXT – GHS7M-1005-6 Mated With GHSM-BSS.....	24
6.2. Time Domain Analysis – GHS7M-1005-6 Mated With GHSM-BSS	25



7.	Performance of Wired Connector GHS7M-1005-6 Mated With Right Angle PC Tail GHSM-HBR	26
7.1.	Frequency Domain Analysis	26
7.1.1.	Insertion Loss – GHS7M-1005-6 Mated With GHSM-HBR	26
7.1.2.	Return Loss – GHS7M-1005-6 Mated With GHSM-HBR	27
7.1.3.	NEXT – GHS7M-1005-6 Mated With GHSM-HBR.....	28
7.1.4.	FEXT – GHS7M-1005-6 Mated With GHSM-HBR	29
7.2.	Time Domain Analysis – GHS7M-1005-6 Mated With GHSM-HBR.....	30
8.	Performance – Wired Connector GHSM (15E) Mated Pair	31
8.1.	Frequency Domain Analysis	31
8.1.1.	Insertion Loss – Wired Connector GHSM (15E) Mated Pair	31
8.1.2.	Return Loss – Wired Connector GHSM (15E) Mated Pair	32
8.1.3.	NEXT – Wired Connector GHSM (15E) Mated Pair.....	33
8.1.4.	FEXT – Wired Connector GHSM (15E) Mated Pair	34
8.2.	Time Domain Analysis – Wired Connector GHSM (15E) Mated Pair.....	35
9.	Performance – FeedThru Connector	36
9.1.	Frequency Domain Analysis	36
9.1.1.	Insertion Loss – FeedThru Connector Pair	36
9.1.2.	Return Loss – FeedThru Connector.....	37
9.1.3.	NEXT – FeedThru Connector.....	38
9.1.4.	FEXT – FeedThru Connector	39
9.2.	Time Domain Analysis – FeedThru Connector	40
10.	Performance – Sav-Con Connector	41
10.1.	Frequency Domain Analysis.....	41
10.1.1.	Insertion Loss – Sav-Con Connector Pair	41
10.1.2.	Return Loss – Sav-Con Connector	42
10.1.3.	NEXT – Sav-Con Connector	43
10.1.4.	FEXT – Sav-Con Connector.....	44
10.2.	Time Domain Analysis – Sav-Con Connector	45



Table of Figures

Figure 1. Straight PC Tail GHSM-BSS Pin and Socket Test PCB's	8
Figure 2. Right Angle PC Tail GHSM-HBR Pin and Socket Test PCB's	9
Figure 3. Cable assembly GHS7M-1005-6	9
Figure 4. Wired Connector GHSM (15E) Mated Pair	9
Figure 5. Wired Connector GHSM (15E) Mated Pair	10
Figure 6. Wired Connector GHSM (15E) Mated Pair	10
Figure 7. GHSM (15E) Pinout for Ethernet Signaling	10
Figure 8. Insertion Loss – GHSM-BSS Mated Pair	11
Figure 9. Return Loss – GHSM-BSS Mated Pair	12
Figure 10. NEXT – GHSM-BSS Mated Pair	13
Figure 11. FEXT – GHSM-BSS Mated Pair	14
Figure 12. TDR – GHSM-BSS Mated Pair	15
Figure 13. Insertion Loss – GHSM-HBR Mated Pair	16
Figure 14. Return Loss – GHSM-HBR Mated Pair	17
Figure 15. NEXT – GHSM-HBR Mated Pair	18
Figure 16. FEXT – GHSM-HBR Mated Pair	19
Figure 17. TDR – GHSM-HBR Mated Pair	20
Figure 18. Insertion Loss – GHS7M-1005-6 Mated With GHSM-BSS	21
Figure 19. Return Loss – GHS7M-1005-6 Mated With GHSM-BSS	22
Figure 20. NEXT – GHS7M-1005-6 Mated With GHSM-BSS	23
Figure 21. FEXT – GHS7M-1005-6 Mated With GHSM-BSS	24
Figure 22. TDR – GHS7M-1005-6 Mated With GHSM-BSS	25
Figure 23. Insertion Loss – GHS7M-1005-6 Mated With GHSM-HBR	26
Figure 24. Return Loss– GHS7M-1005-6 Mated With GHSM-HBR	27
Figure 25. NEXT– GHS7M-1005-6 Mated With GHSM-HBR	28
Figure 26. FEXT– GHS7M-1005-6 Mated With GHSM-HBR	29
Figure 27. TDR– GHS7M-1005-6 Mated With GHSM-HBR	30
Figure 28. Insertion Loss – Wired Connector GHSM (15E) Mated Pair	31
Figure 29. Return Loss – Wired Connector GHSM (15E) Mated Pair	32
Figure 30. NEXT – Wired Connector GHSM (15E) Mated Pair	33
Figure 31. FEXT – Wired Connector GHSM (15E) Mated Pair	34
Figure 32. TDR – Wired Connector GHSM (15E) Mated Pair	35
Figure 33. Insertion Loss – FeedThru Connector	36
Figure 34. Return Loss – FeedThru Connector	37
Figure 35. NEXT – FeedThru Connector	38
Figure 36. FEXT – FeedThru Connector	39
Figure 37. TDR – FeedThru Connector	40
Figure 38. Insertion Loss – Sav-Con Connector	41



Figure 39. Return Loss – Sav-Con Connector42
Figure 40. NEXT – Sav-Con Connector43
Figure 41. FEXT – Sav-Con Connector44
Figure 42. TDR – Sav-Con Connector45



1. Introduction

This document contains results from testing that was performed to evaluate the high-frequency electrical performance of the Glenair High-Speed Micro-D (GHSM) with respect to Ethernet applications. This report outlines frequency domain performance metrics such as insertion loss (IL) and return loss (RL) as well as the time-domain performance metric of impedance.

For S-Parameter models of the results shown in this test report, refer to [AN0024](#).

2. Product Overview

High-speed datalink applications such as aircraft avionics and other high data rate and bandwidth equipment require both optimized data transmission performance as well as robust mechanical and EMC performance. Micro-D connector packaging with high-retention-force TwistPin contacts has a proven track record in standard signal and power applications. The Glenair High-Speed Micro-D (GHSM) brings high-speed datalink performance to these mission-critical platforms. The GHSM is a 1 Amp pre-wired cable and PCB solution with 10+ Gb/s. performance per differential pair. Auxiliary EMC ground springs on plug and integral contact separation architecture ensures data integrity and low attenuation performance.

3. Test Setup

This section details the test assemblies, test PCBs and equipment used to perform the high-speed characterization. All measurements were taken using a Tektronix DSA8300 Digital Serial Analyzer and a Keysight N5227B PNA network analyzer which were connected to coaxial-launch test fixture PCBs designed specifically for this testing.

3.1. Test Fixtures

3.1.1. Test Assemblies

Test fixture PCB sets utilizing surface-mount coax connectors were designed for the high-speed tests. Each set consisted of two GHSM to coax boards and a calibration board. One test set used straight PC tail GHSM-BSS series PCB-mount connectors, part numbers GHSM2R-15SBSSPU and GHSM2R-15PBSSLU. The other set used right-angle PC tail GHSM-HBR series PCB-mount connectors, part numbers GHSM2R-15PHBRLT-.110 and GHSM2R-15SHBRPT-.110. Photographs of the test boards are seen in the following two figures.

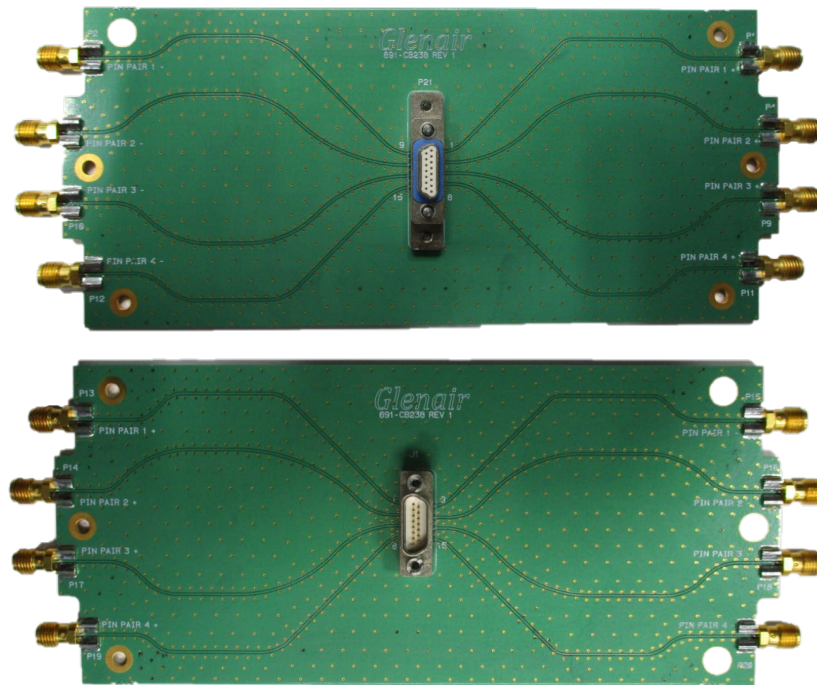


Figure 1. Straight PC Tail GHSM-BSS Pin and Socket Test PCB's

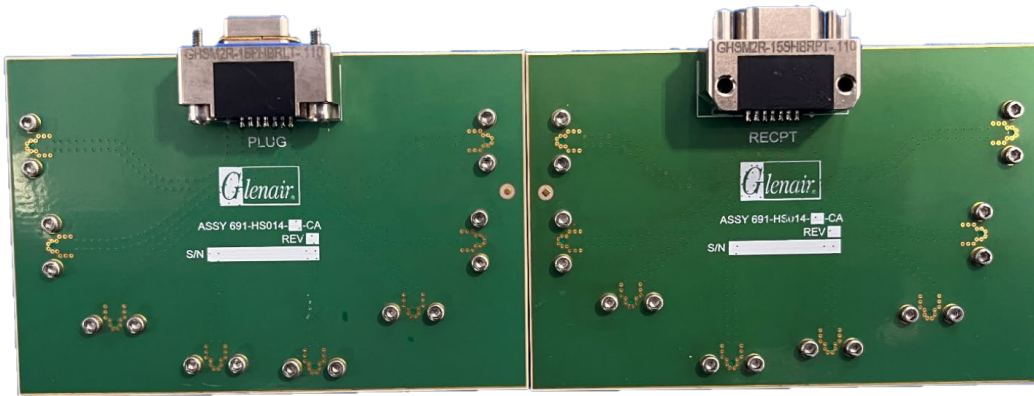


Figure 2. Right Angle PC Tail GHSM-HBR Pin and Socket Test PCB's

The board sets were manufactured as a single panel and separated into individual test boards to give consistent signal characteristics.

Cable assembly GHS7M-1005-6 was added between test PCBs to measure results including cable assembly. See Figure 3 below. Test results for this assembly are in Sections 6 and 7.

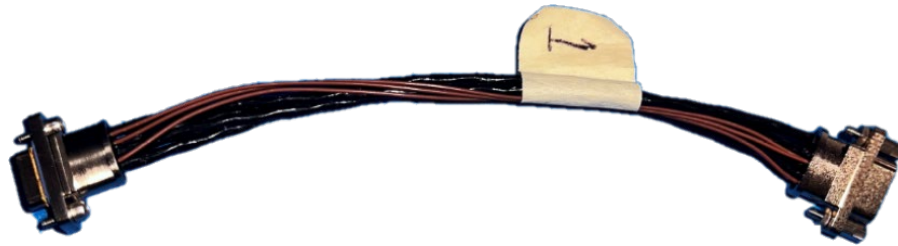


Figure 3. Cable assembly GHS7M-1005-6

The final cable assembly test piece consisted of GHSM2R-15EP-A-6 and GHSM2R-15ES-A-6 along with test interface PCB's. The test interface PCB's and lead-in cables were de-embedded to provide mated connector results only. See Figure 4 below. Test results for this assembly are in Section 8.



Figure 4. Wired Connector GHSM (15E) Mated Pair

The Feed-Thru connector, GHSM-1011-2R15SN, was inserted into the cable assembly of Figure 4 and tested.



Figure 5. Feed-Thru Connector

The Sav-Con connector, GHSM2R-15USP1, was also inserted into the cable assembly of Figure 4 and tested.



Figure 6. Sav-Con Connector

3.2. Test Pairs

Figure 7 shows the test pair arrangement.

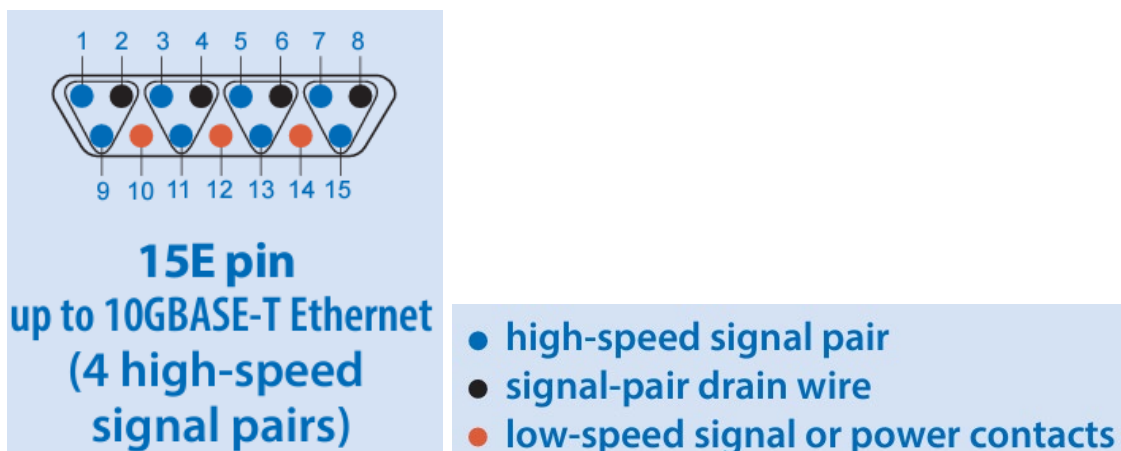


Figure 7. GHSM (15E) Pinout for Ethernet Signaling

4. Performance of Straight PC Tail GHSM-BSS Mated Pair

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

4.1. Frequency Domain Analysis

4.1.1. Insertion Loss – GHSM-BSS Mated Pair

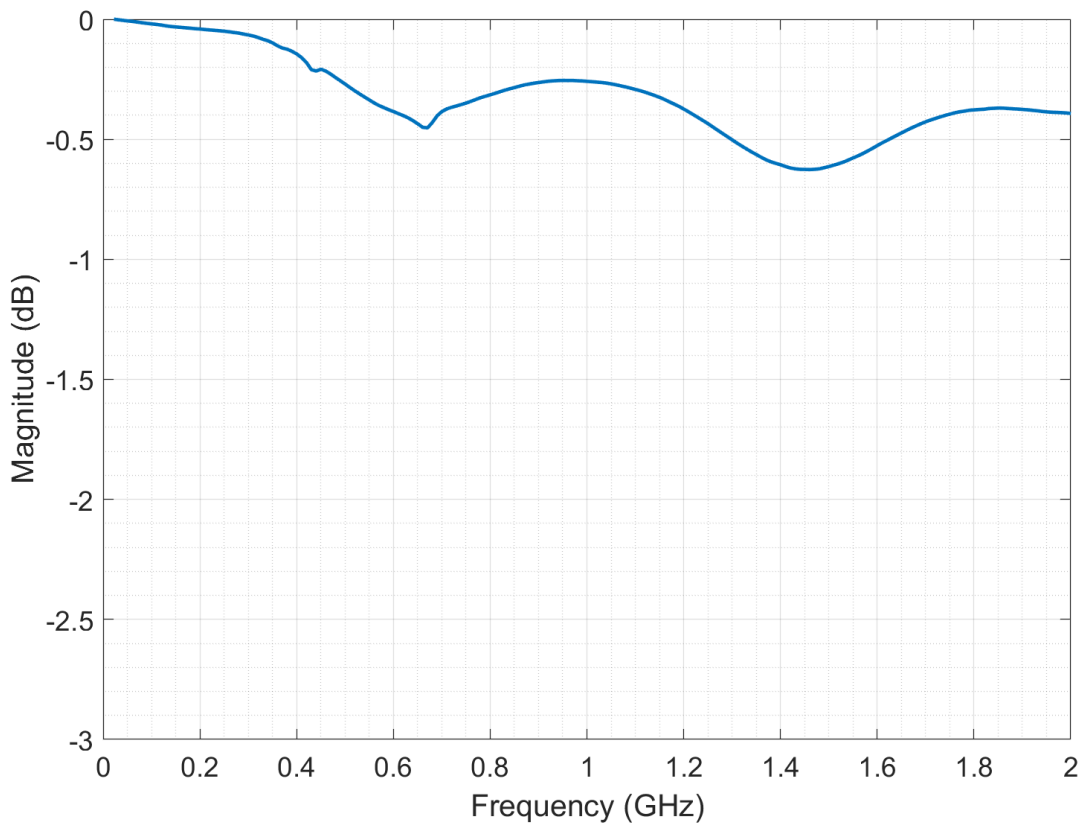


Figure 8. Insertion Loss – GHSM-BSS Mated Pair

4.1.2. Return Loss - GHSM-BSS Mated Pair

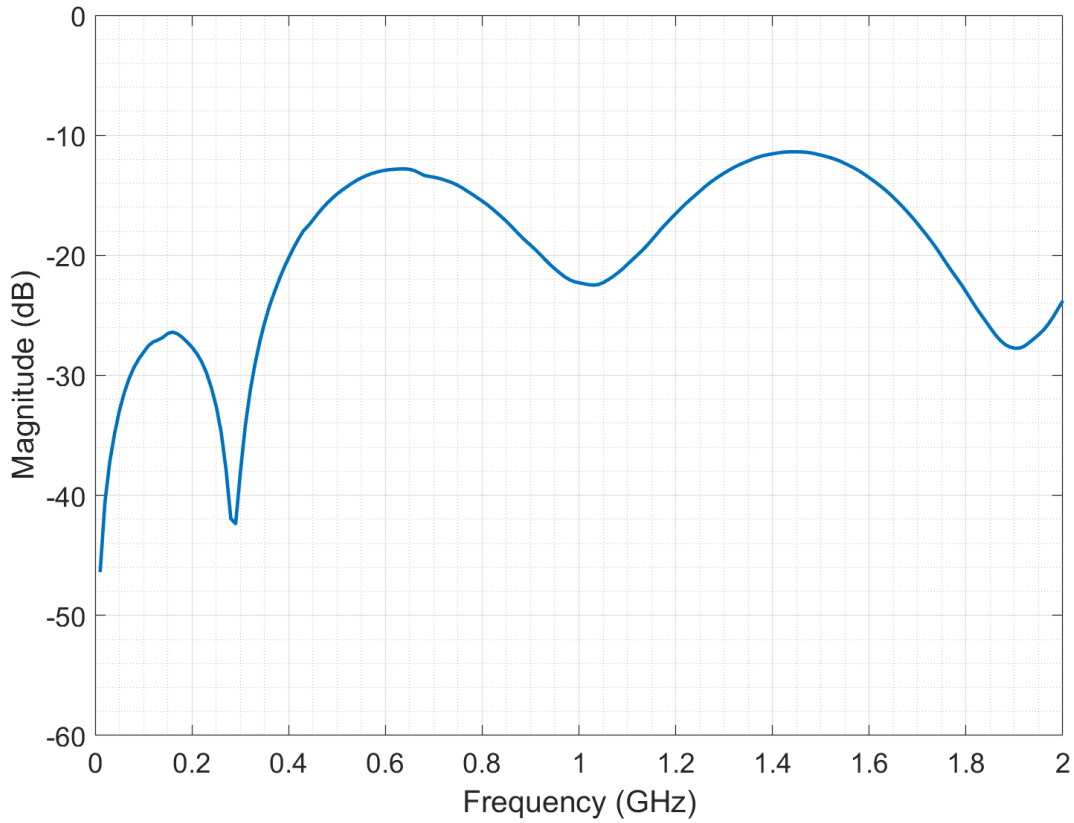


Figure 9. Return Loss – GHSM-BSS Mated Pair

4.1.3. NEXT - GHSM-BSS Mated Pair

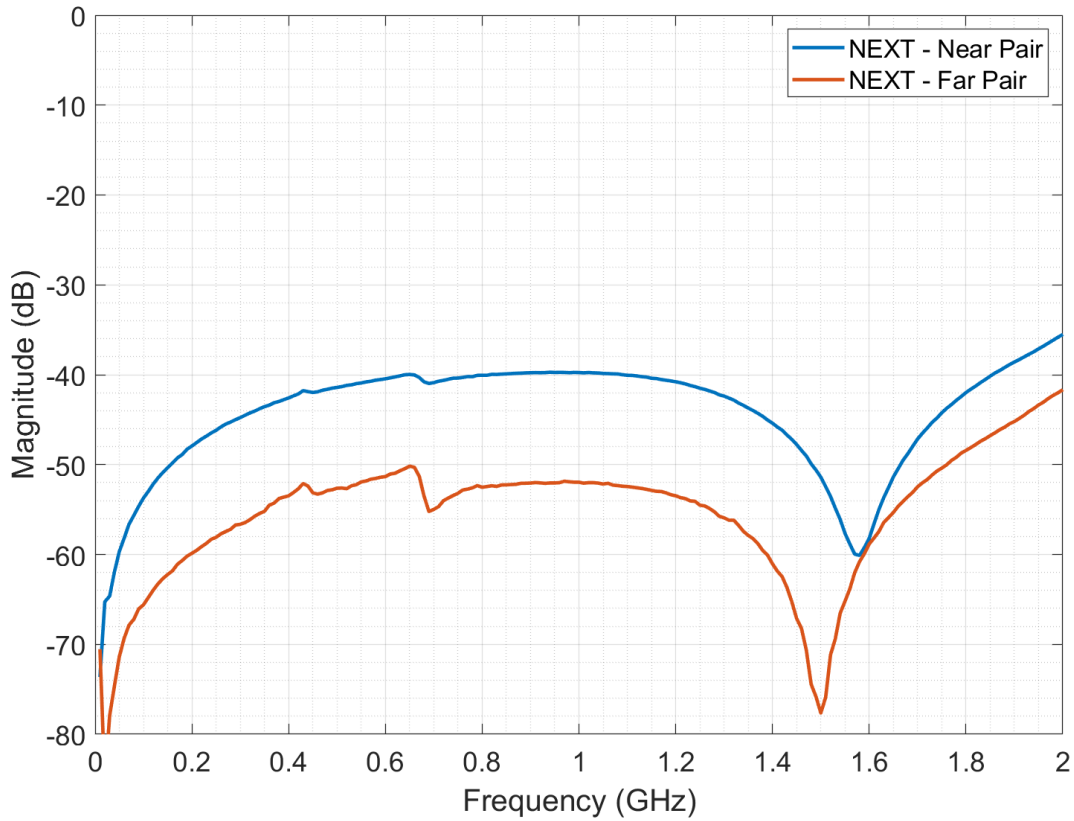


Figure 10. NEXT – GHSM-BSS Mated Pair

4.1.4. FEXT - GHSM-BSS Mated Pair

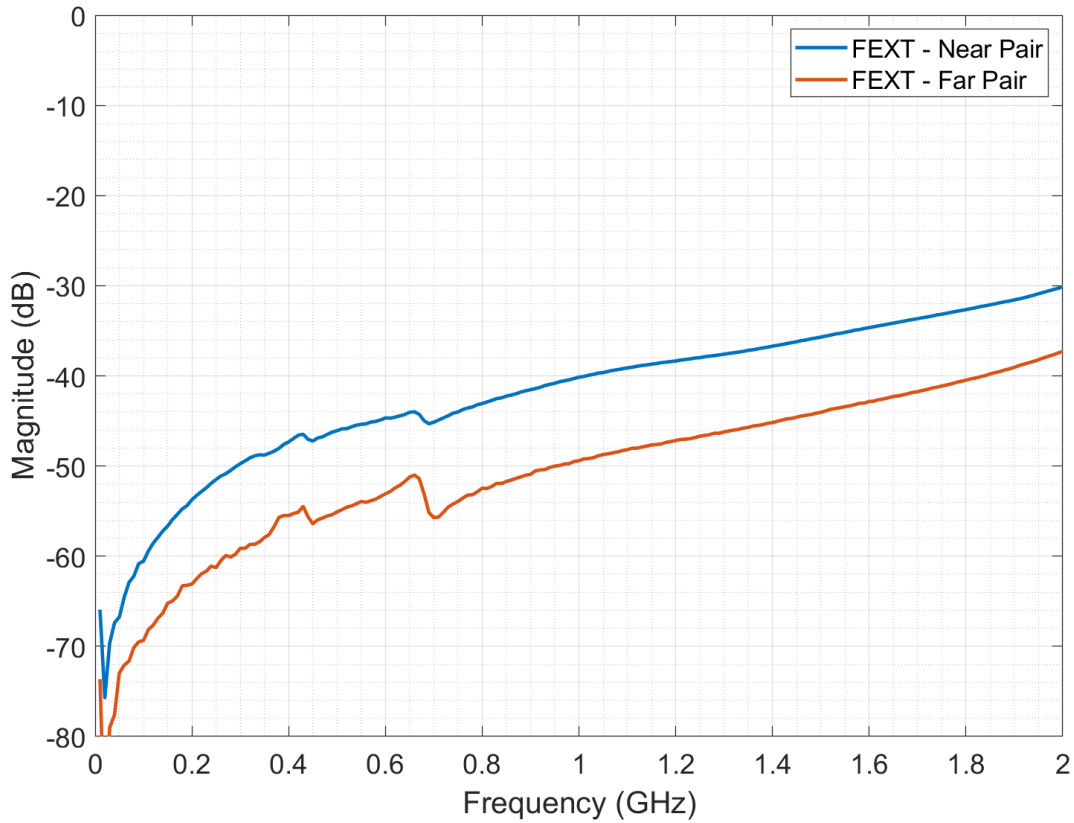


Figure 11. FEXT – GHSM-BSS Mated Pair

4.2. Time Domain Analysis - GHSM-BSS Mated Pair

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. Rise times of 100ps, and 200ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
100	3.5
200	1.75

Table 1. Bandwidth to Rise Time Relationship

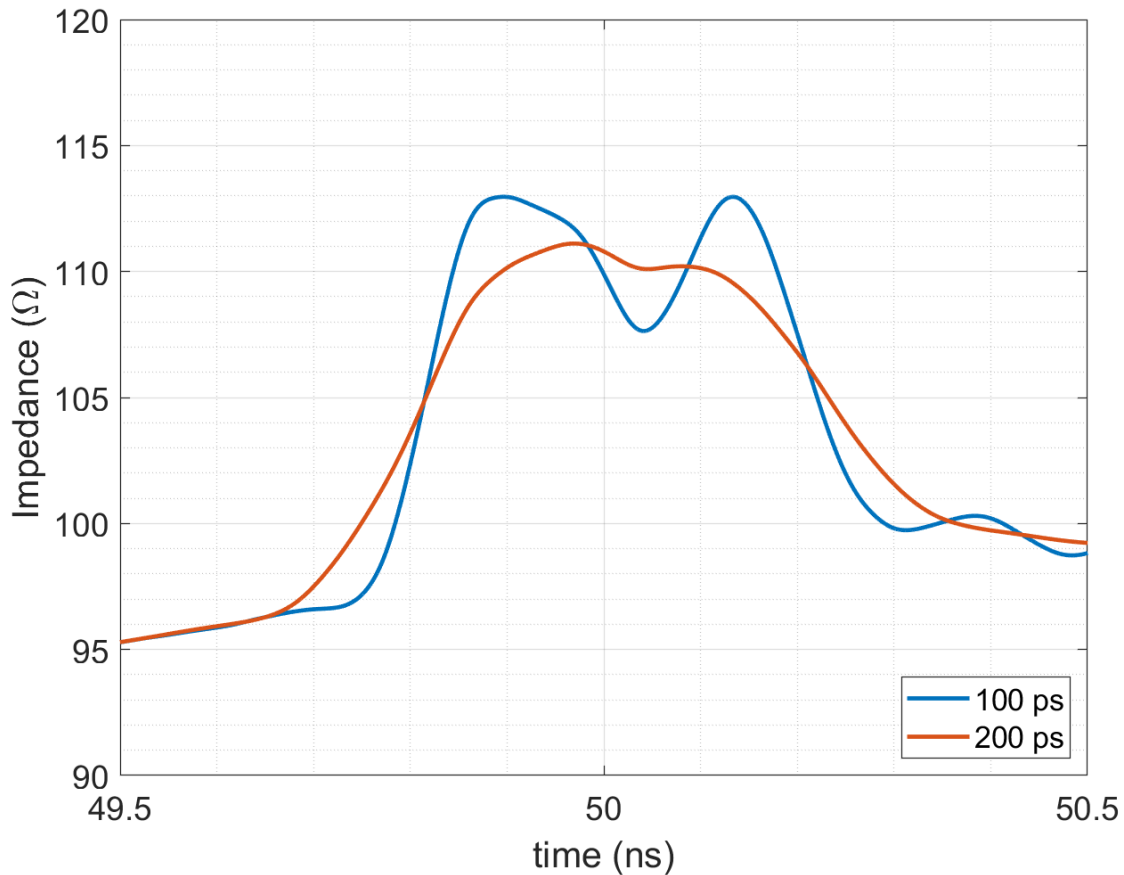


Figure 12. TDR – GHSM-BSS Mated Pair

5. Performance of Right-Angle PC Tail GHSM-HBR Mated Pair

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

5.1. Frequency Domain Analysis

5.1.1. Insertion Loss – GHSM-HBR Mated Pair

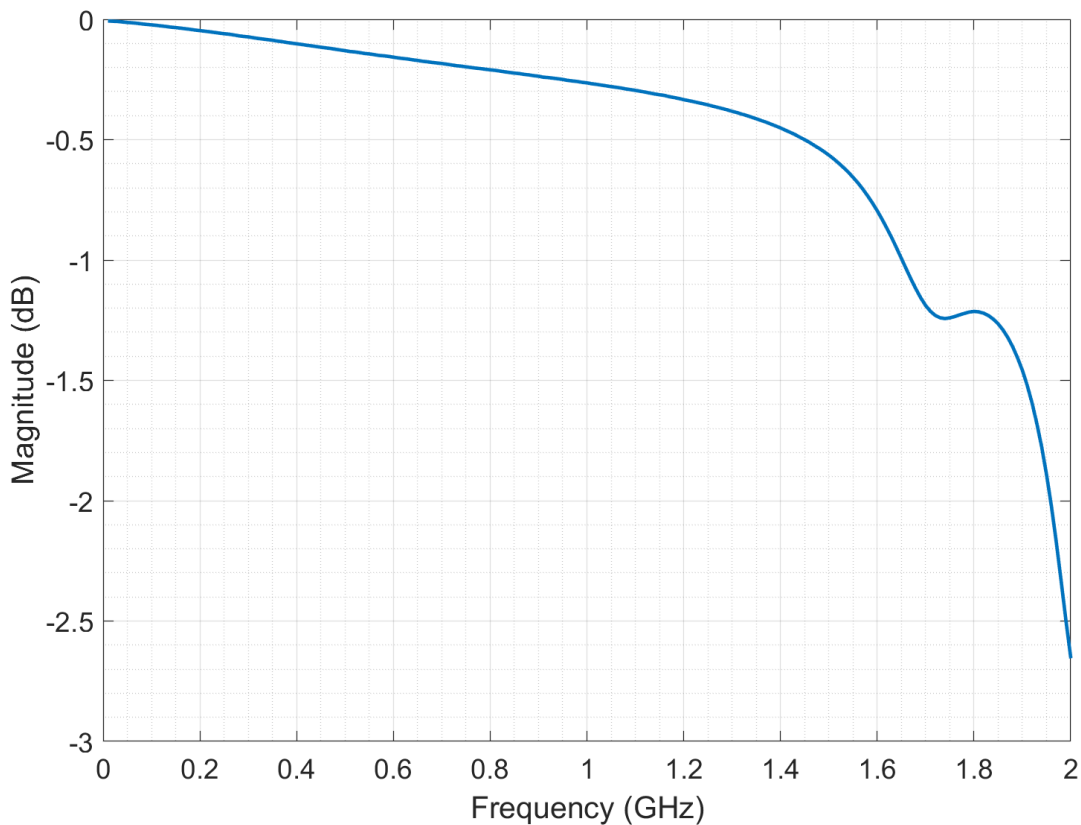


Figure 13. Insertion Loss – GHSM-HBR Mated Pair

5.1.2. Return Loss – GHSM-HBR Mated Pair

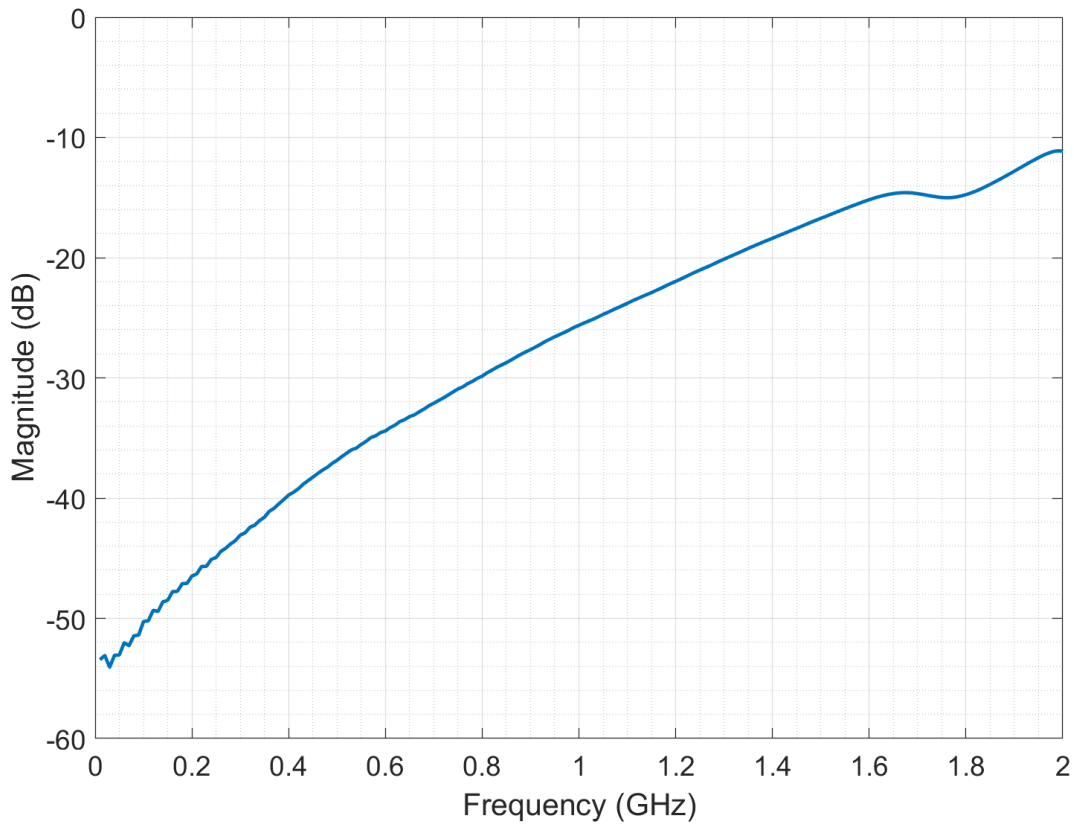


Figure 14. Return Loss – GHSM-HBR Mated Pair

5.1.3. NEXT- GHSM-HBR Mated Pair

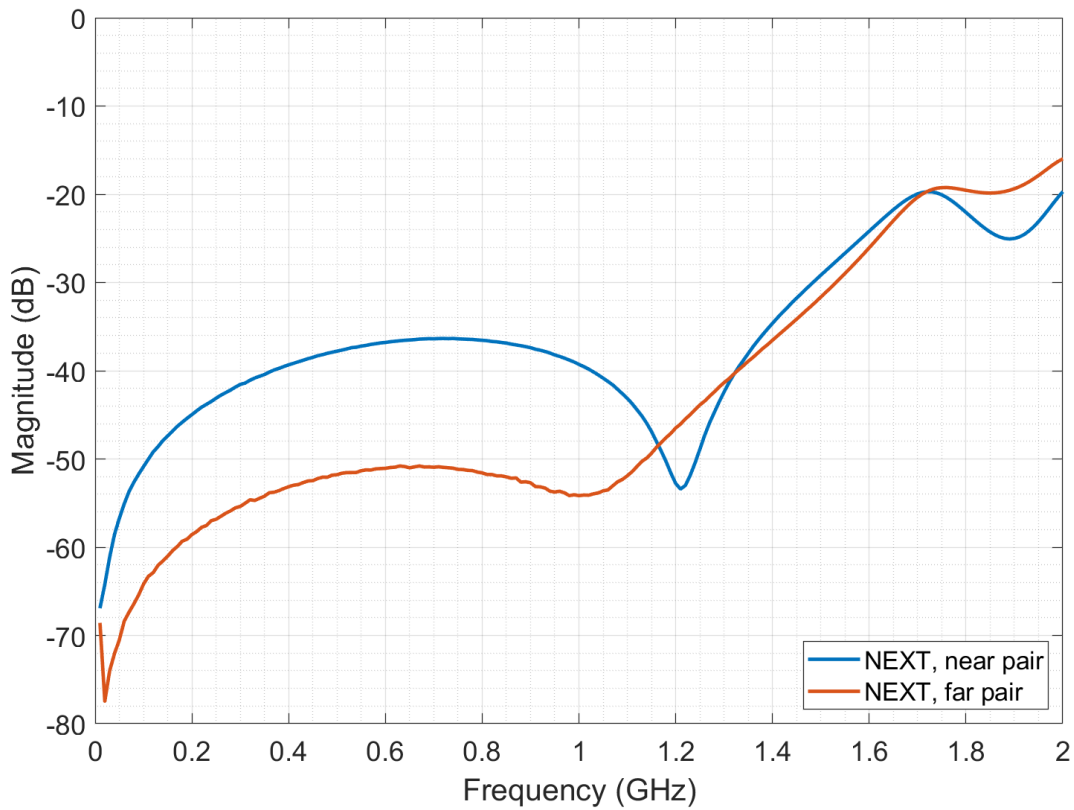


Figure 15. NEXT – GHSM-HBR Mated Pair

5.1.4. FEXT – GHSM-HBR Mated Pair

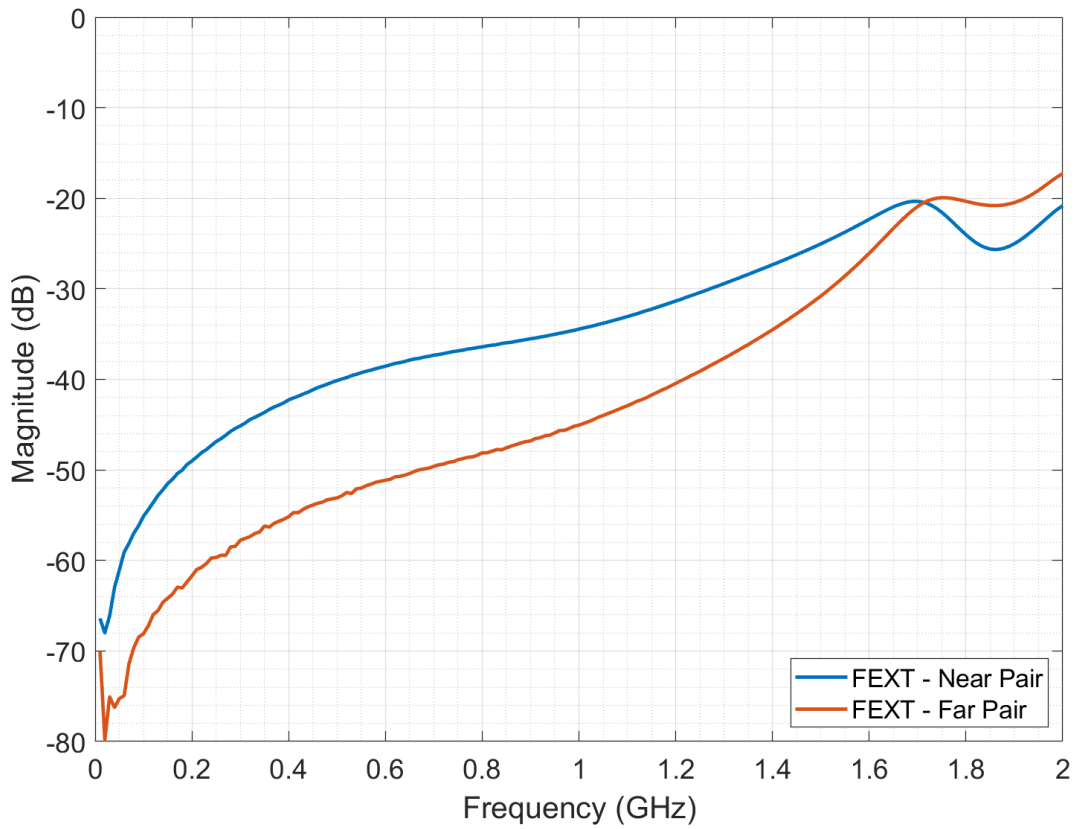


Figure 16. FEXT – GHSM-HBR Mated Pair

5.2. Time Domain Analysis – GHSM-HBR Mated Pair

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal’s rising edge. Rise times of 100 ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

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200	1.75

Table 1. Bandwidth to Rise Time Relationship

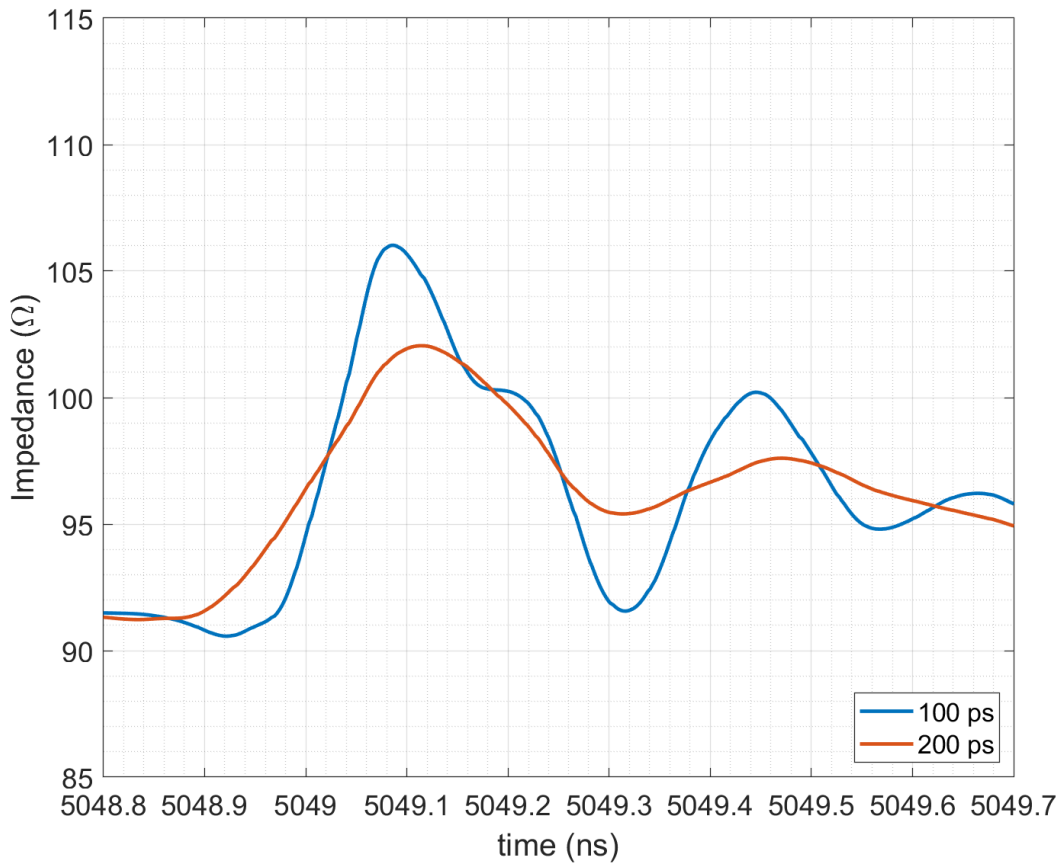


Figure 17. TDR – GHSM-HBR Mated Pair

6. Performance of Wired Connector GHS7M-1005-6 Mated With Straight PC Tail GHSM-BSS

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

6.1. Frequency Domain Analysis

6.1.1. Insertion Loss – GHS7M-1005-6 Mated With GHSM-BSS

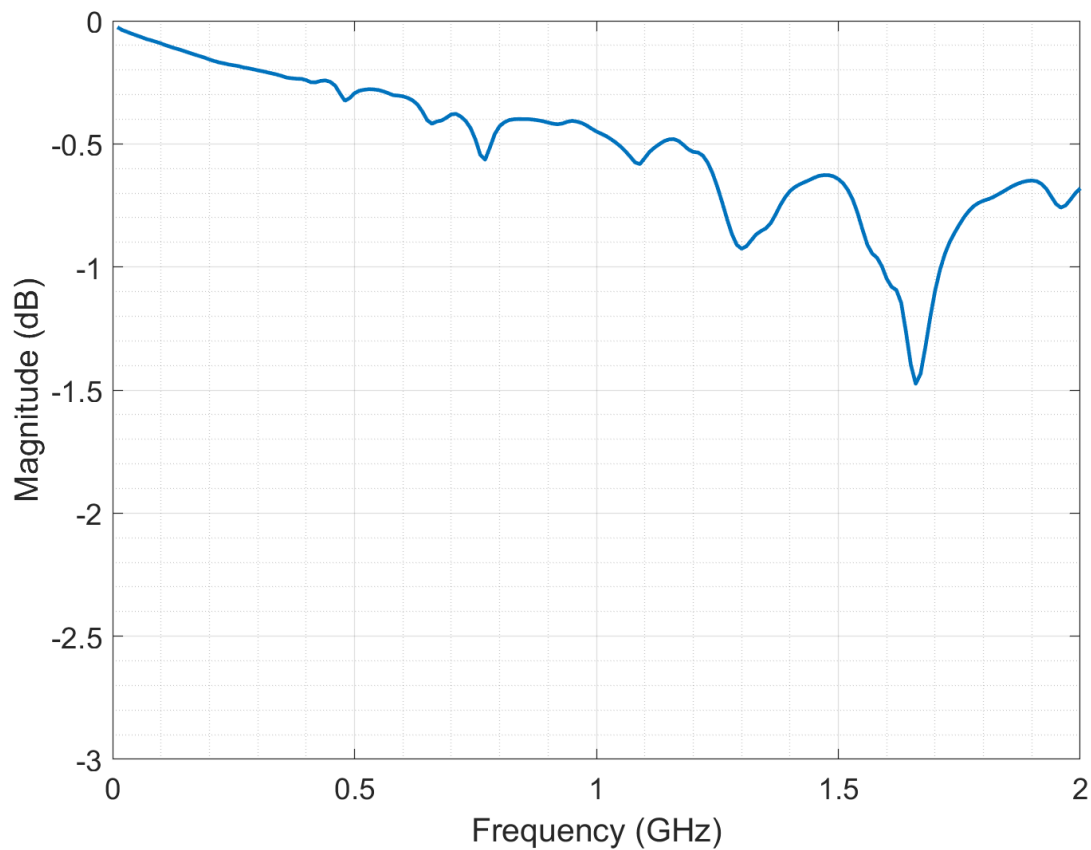


Figure 18. Insertion Loss – GHS7M-1005-6 Mated With GHSM-BSS

6.1.2. Return Loss - GHS7M-1005-6 Mated With GHSM-BSS

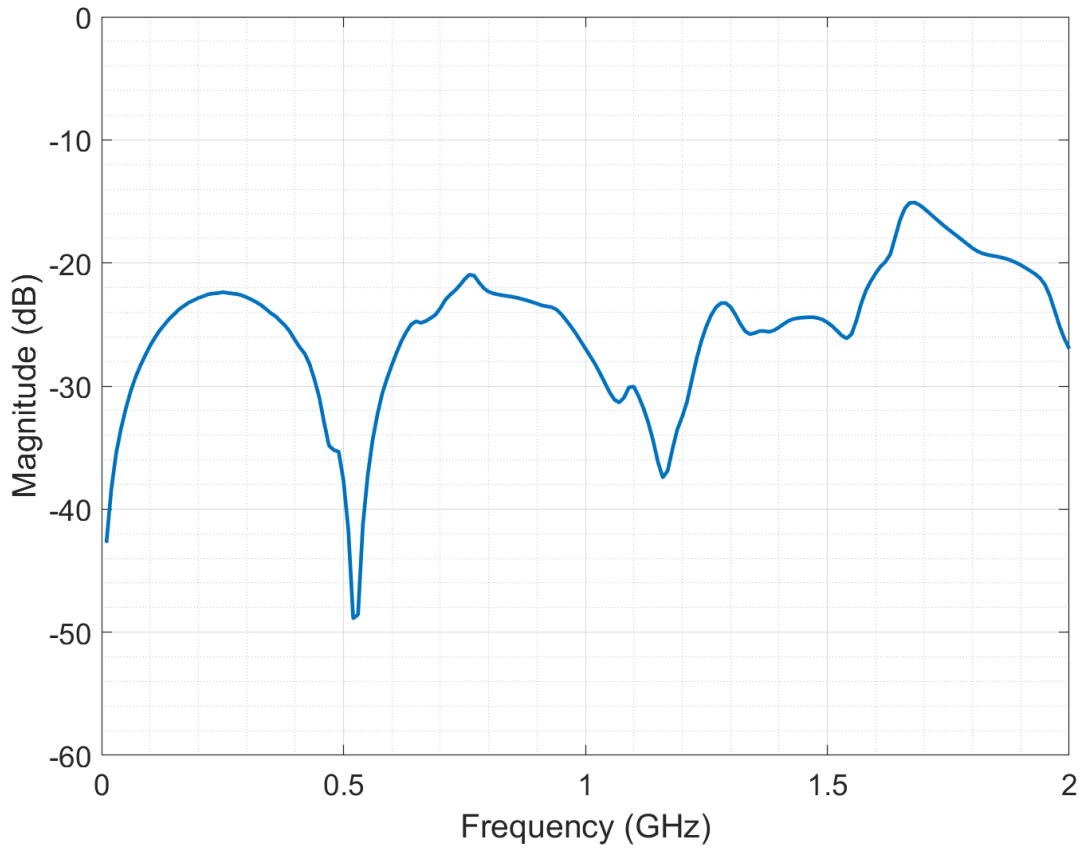


Figure 19. Return Loss – GHS7M-1005-6 Mated With GHSM-BSS

6.1.3. NEXT – GHS7M-1005-6 Mated With GHSM-BSS

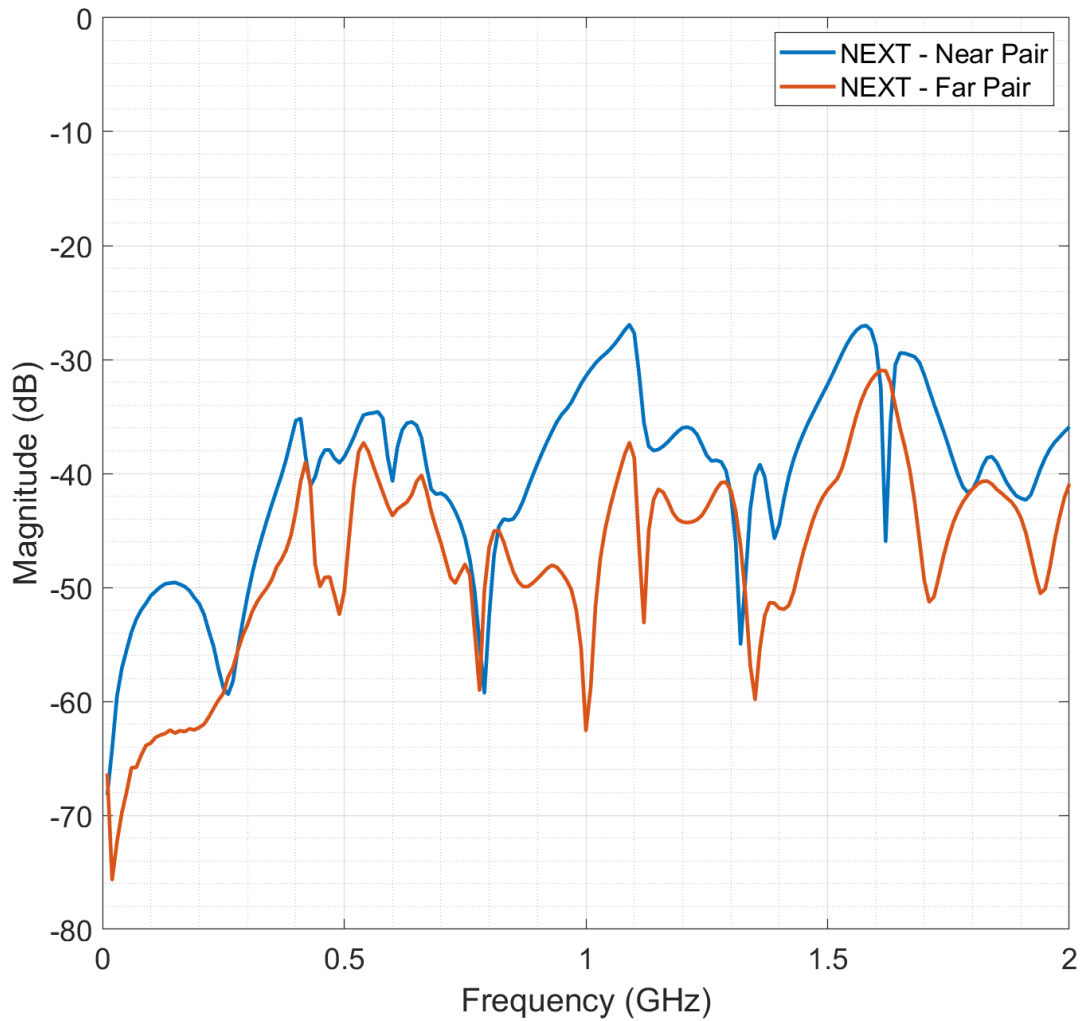


Figure 20. NEXT – GHS7M-1005-6 Mated With GHSM-BSS

6.1.4. FEXT – GHS7M-1005-6 Mated With GHSM-BSS

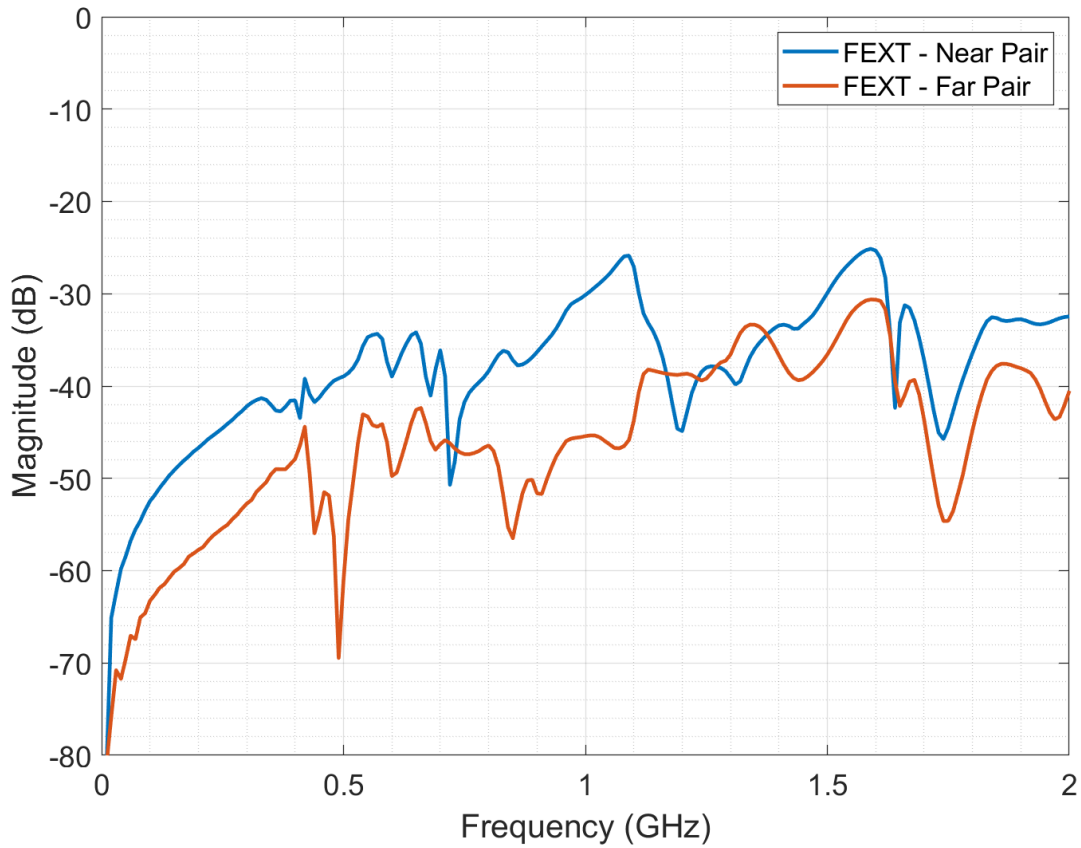


Figure 21. FEXT – GHS7M-1005-6 Mated With GHSM-BSS

6.2. Time Domain Analysis – GHS7M-1005-6 Mated With GHSM-BSS

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal's rising edge. Rise times of 100 ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

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Table 1. Bandwidth to Rise Time Relationship

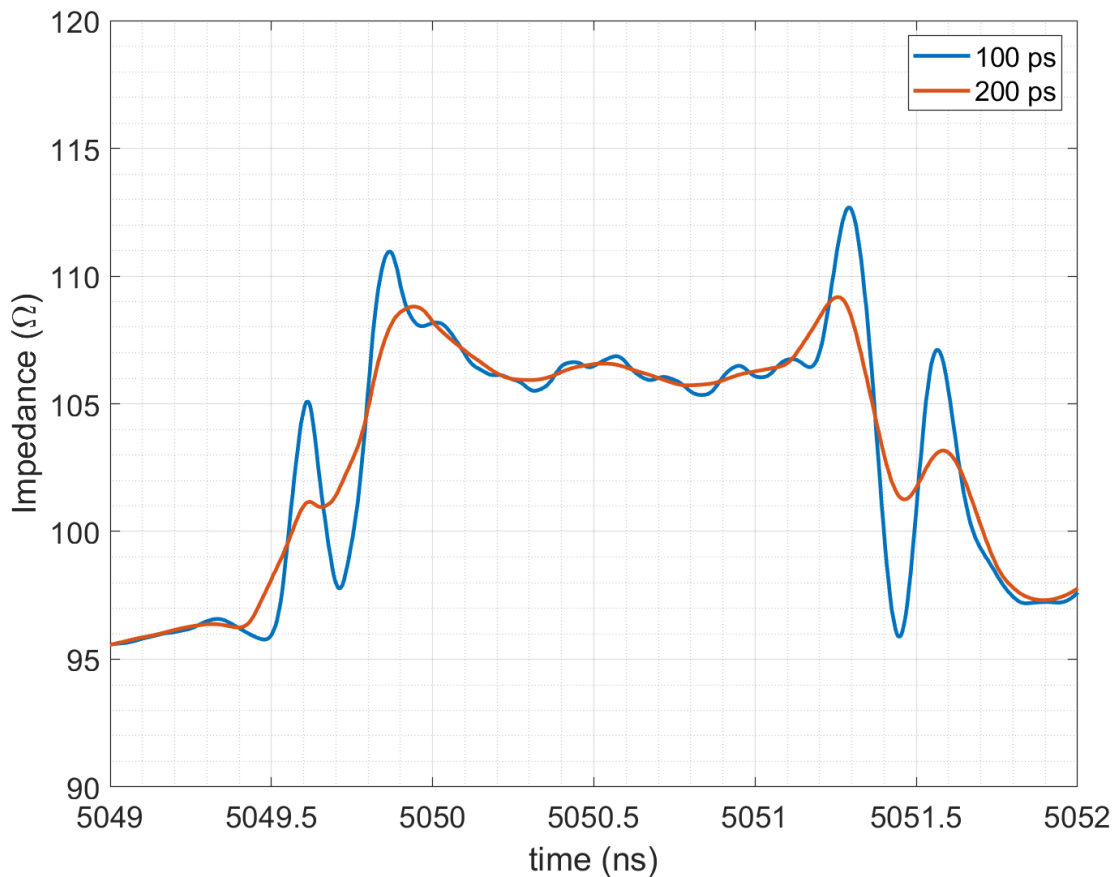


Figure 22. TDR – GHS7M-1005-6 Mated With GHSM-BSS

7. Performance of Wired Connector GHS7M-1005-6 Mated With Right Angle PC Tail GHSM-HBR

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

7.1. Frequency Domain Analysis

7.1.1. Insertion Loss – GHS7M-1005-6 Mated With GHSM-HBR

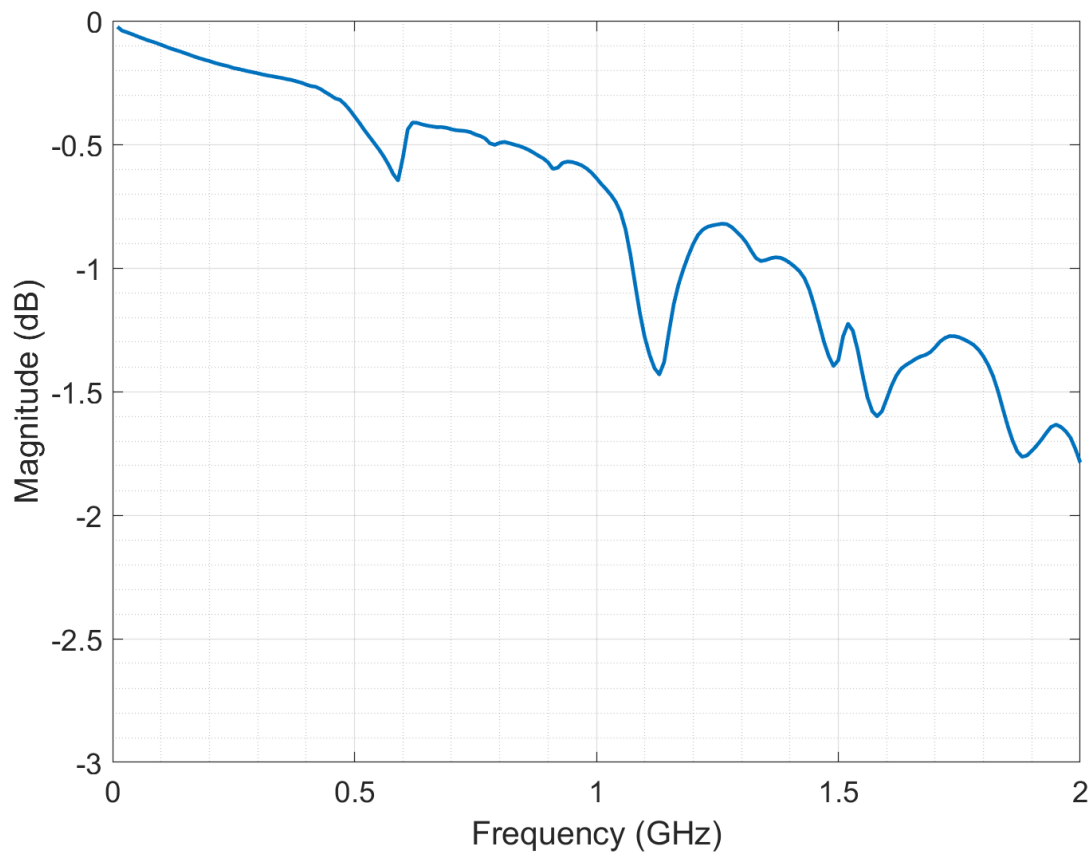


Figure 23. Insertion Loss – GHS7M-1005-6 Mated With GHSM-HBR

7.1.2. Return Loss – GHS7M-1005-6 Mated With GHSM-HBR

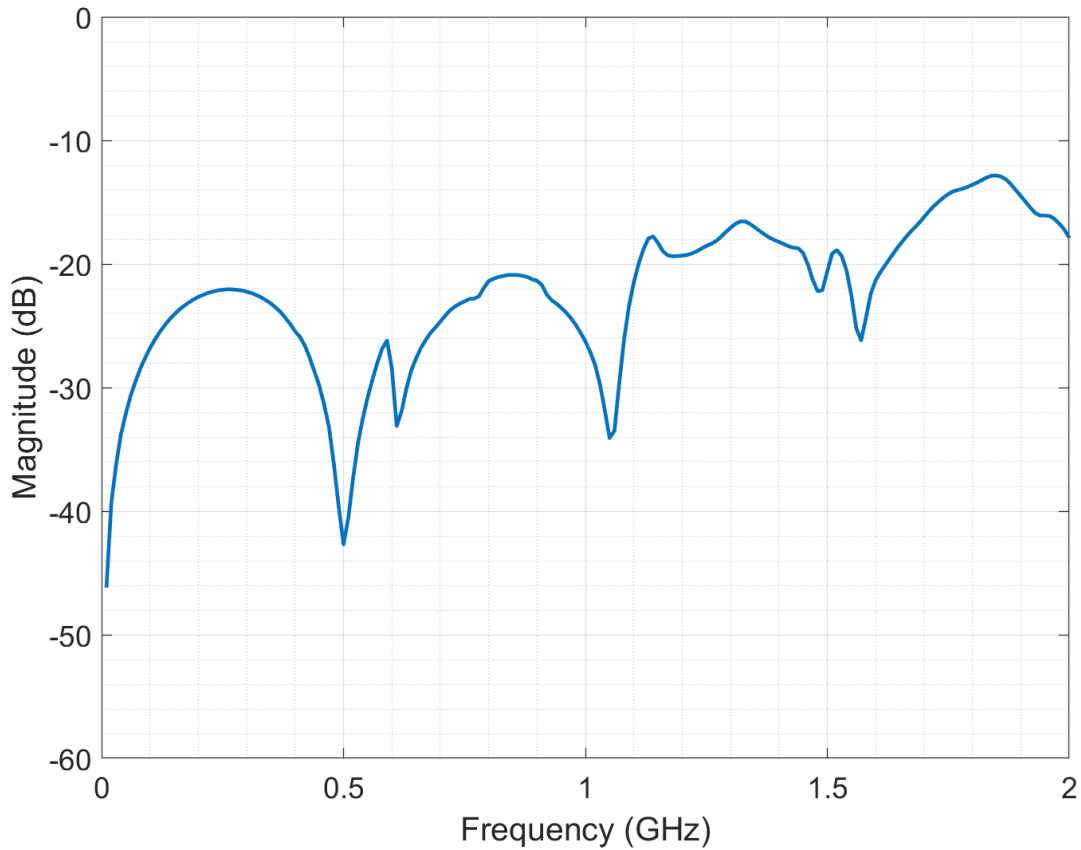


Figure 24. Return Loss– GHS7M-1005-6 Mated With GHSM-HBR

7.1.3. NEXT – GHS7M-1005-6 Mated With GHSM-HBR

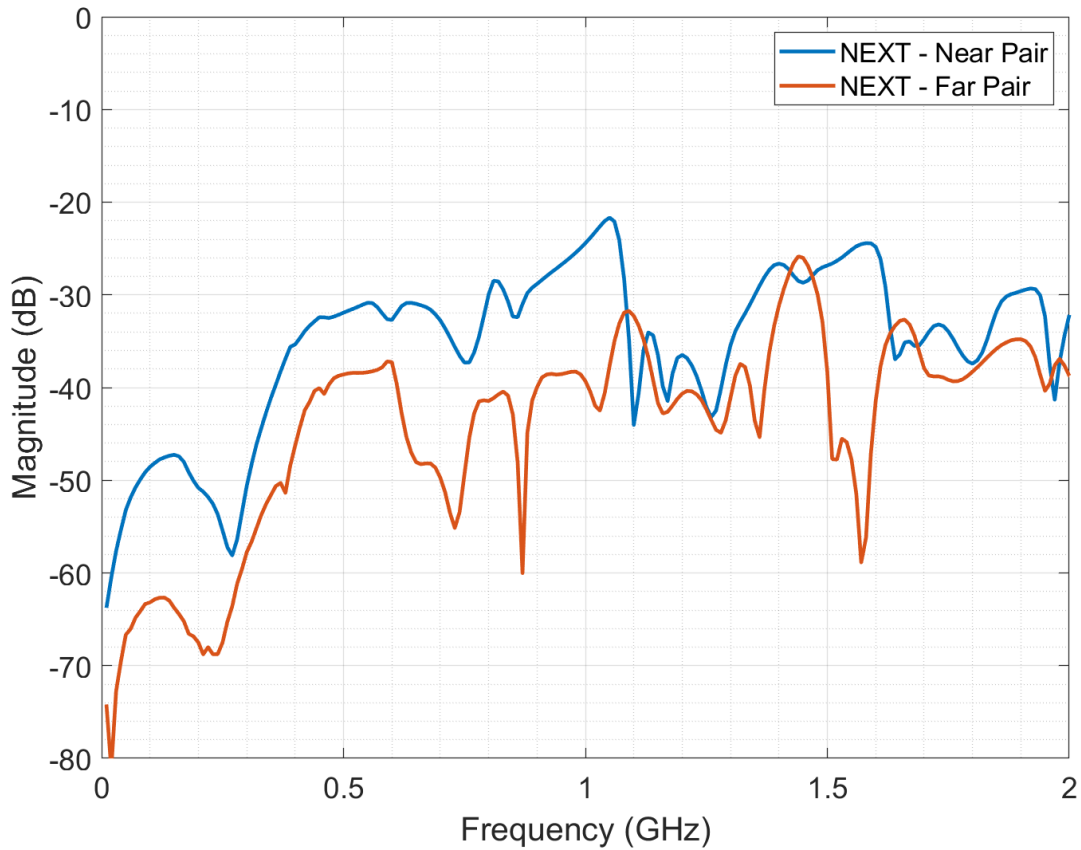


Figure 25. NEXT– GHS7M-1005-6 Mated With GHSM-HBR

7.1.4. FEXT – GHS7M-1005-6 Mated With GHSM-HBR

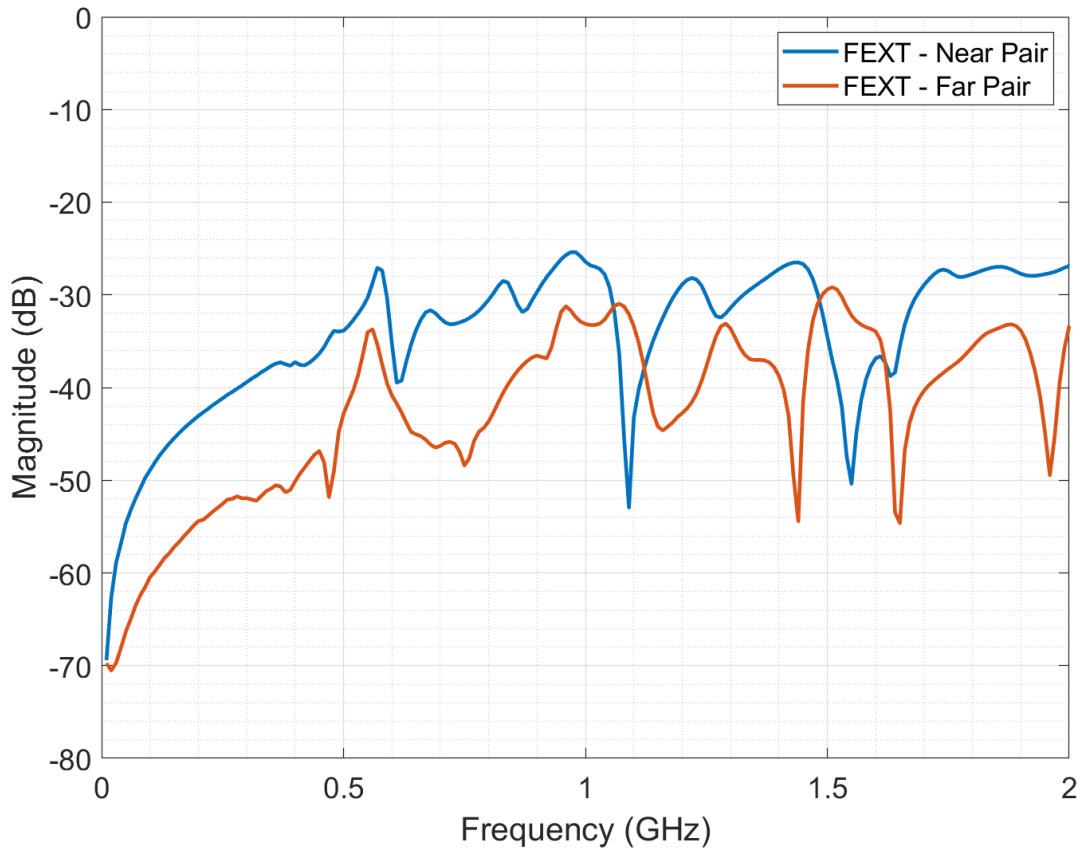


Figure 26. FEXT– GHS7M-1005-6 Mated With GHSM-HBR

7.2. Time Domain Analysis – GHS7M-1005-6 Mated With GHSM-HBR

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal’s rising edge. Rise times of 100 ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
100	3.5
200	1.75

Table 1. Bandwidth to Rise Time Relationship

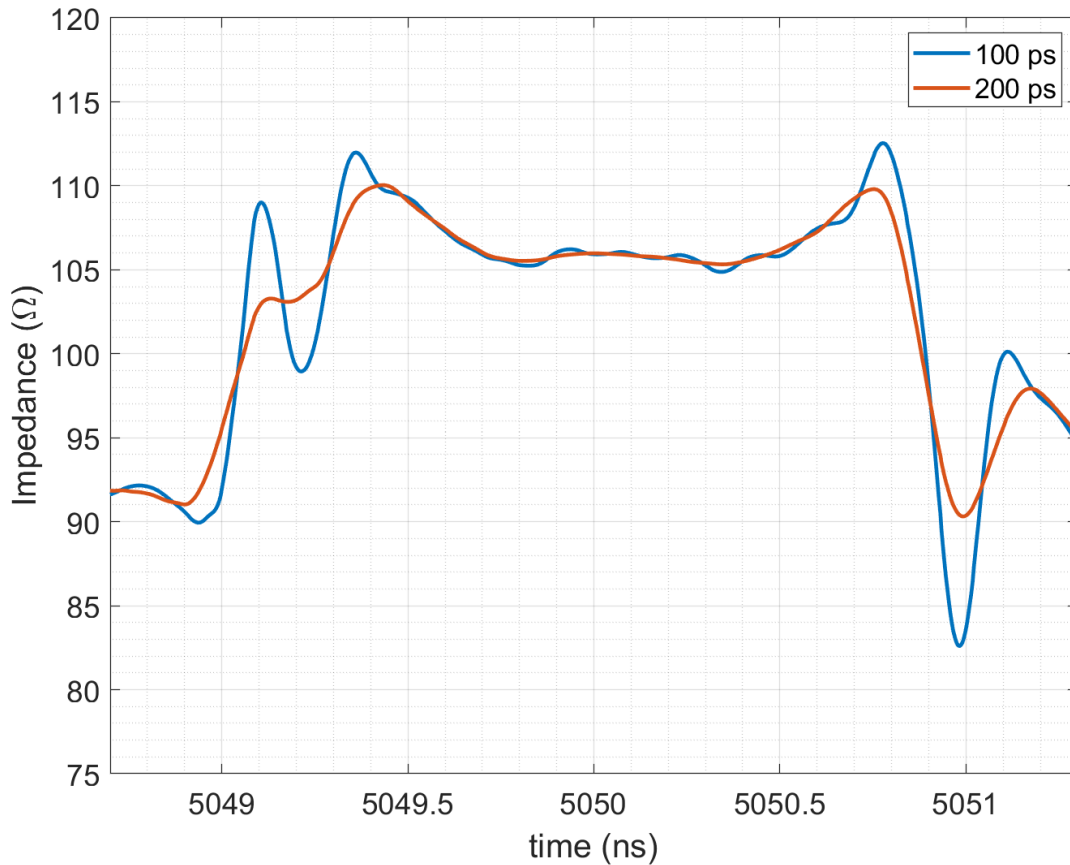


Figure 27. TDR– GHS7M-1005-6 Mated With GHSM-HBR

8. Performance – Wired Connector GHSM (15E) Mated Pair

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

8.1. Frequency Domain Analysis

8.1.1. Insertion Loss – Wired Connector GHSM (15E) Mated Pair

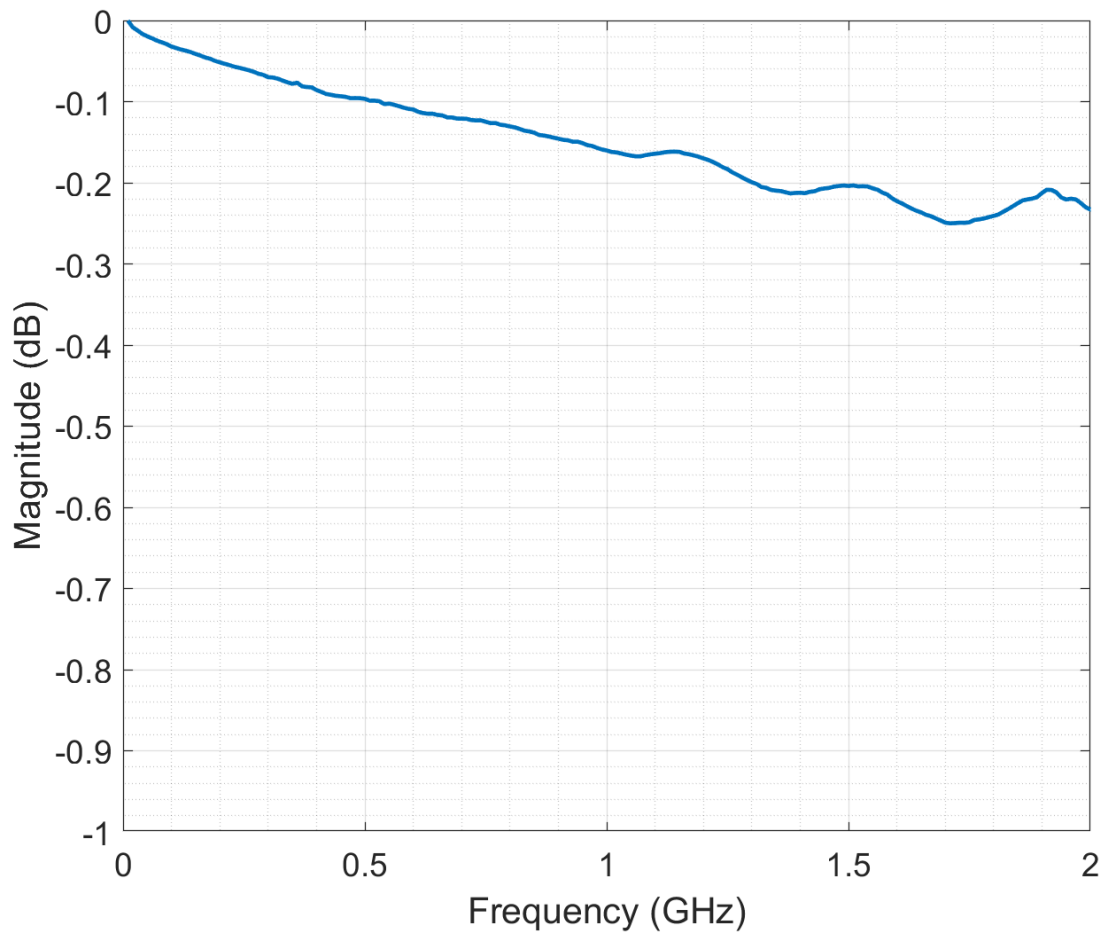


Figure 28. Insertion Loss – Wired Connector GHSM (15E) Mated Pair

8.1.2. Return Loss – Wired Connector GHSM (15E) Mated Pair

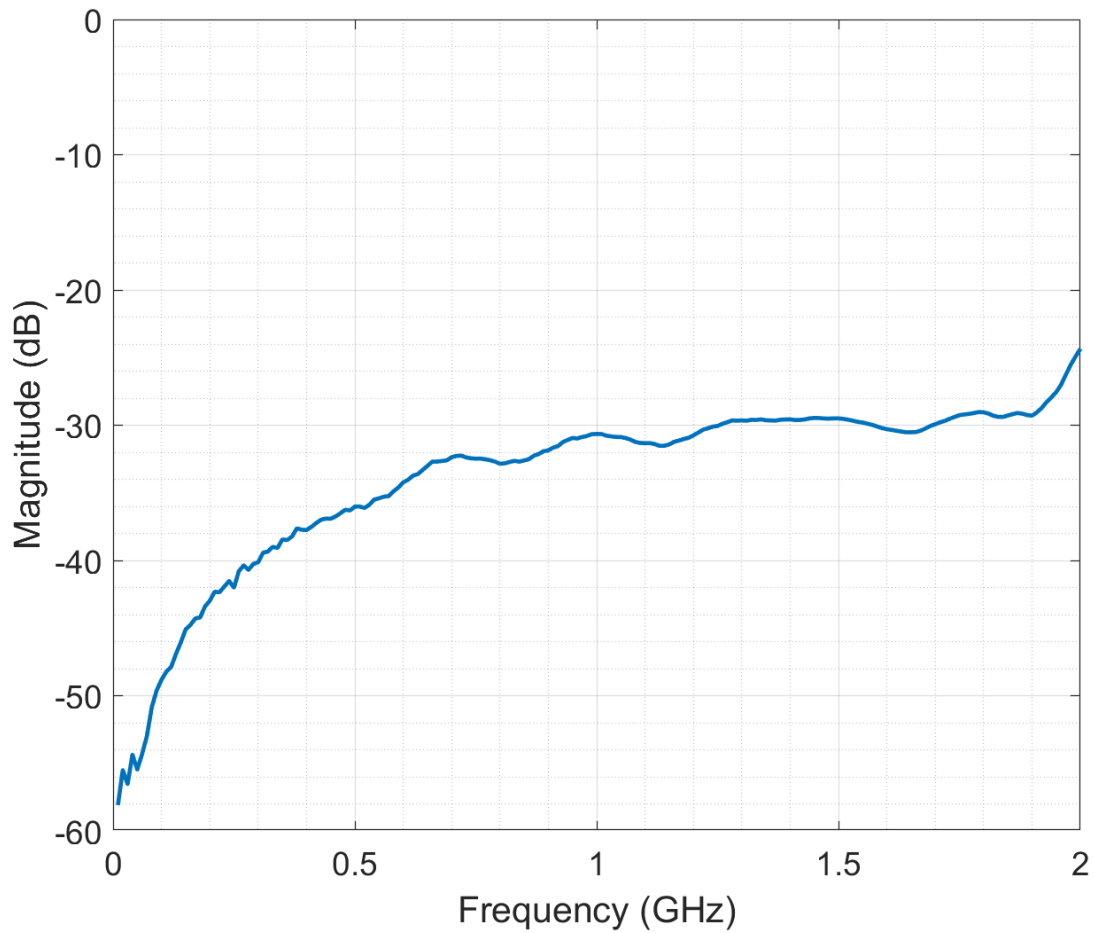


Figure 29. Return Loss – Wired Connector GHSM (15E) Mated Pair

8.1.3. NEXT – Wired Connector GHSM (15E) Mated Pair

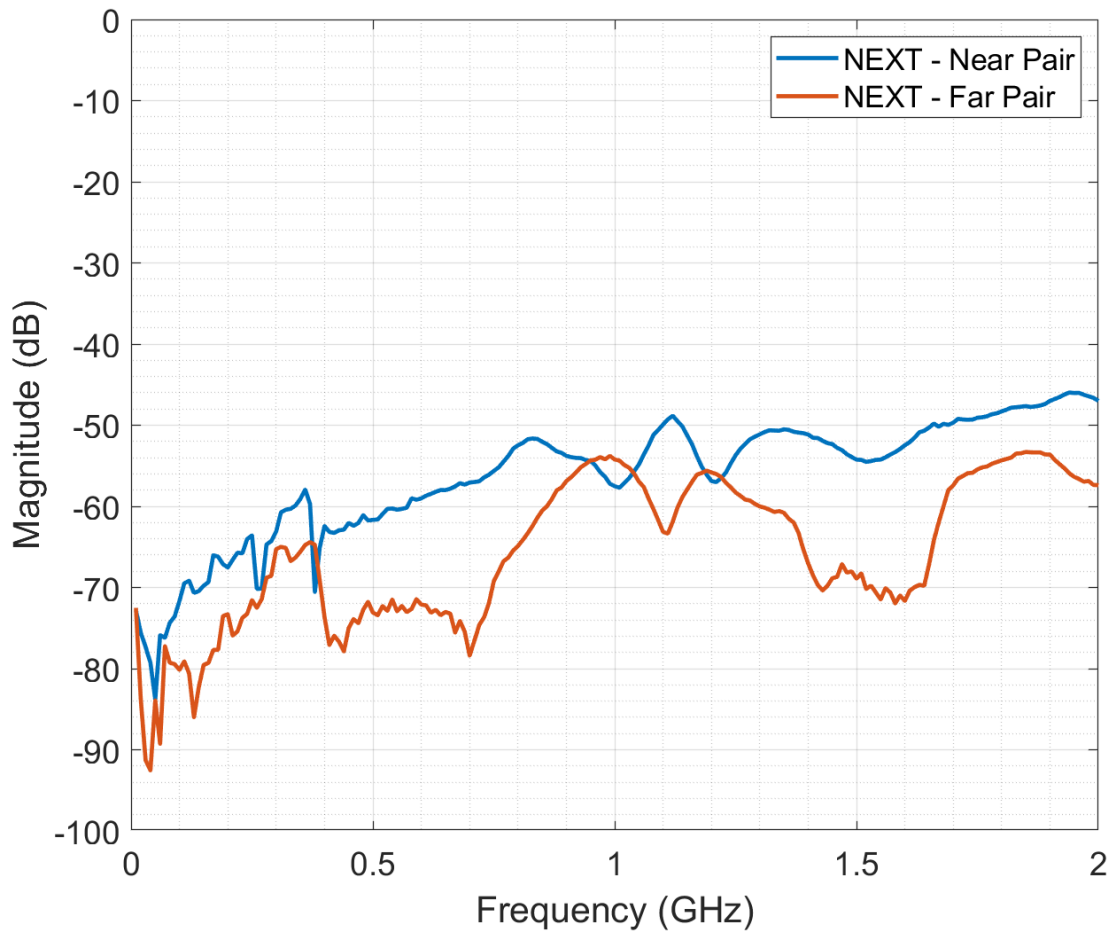


Figure 30. NEXT – Wired Connector GHSM (15E) Mated Pair

8.1.4. FEXT – Wired Connector GHSM (15E) Mated Pair

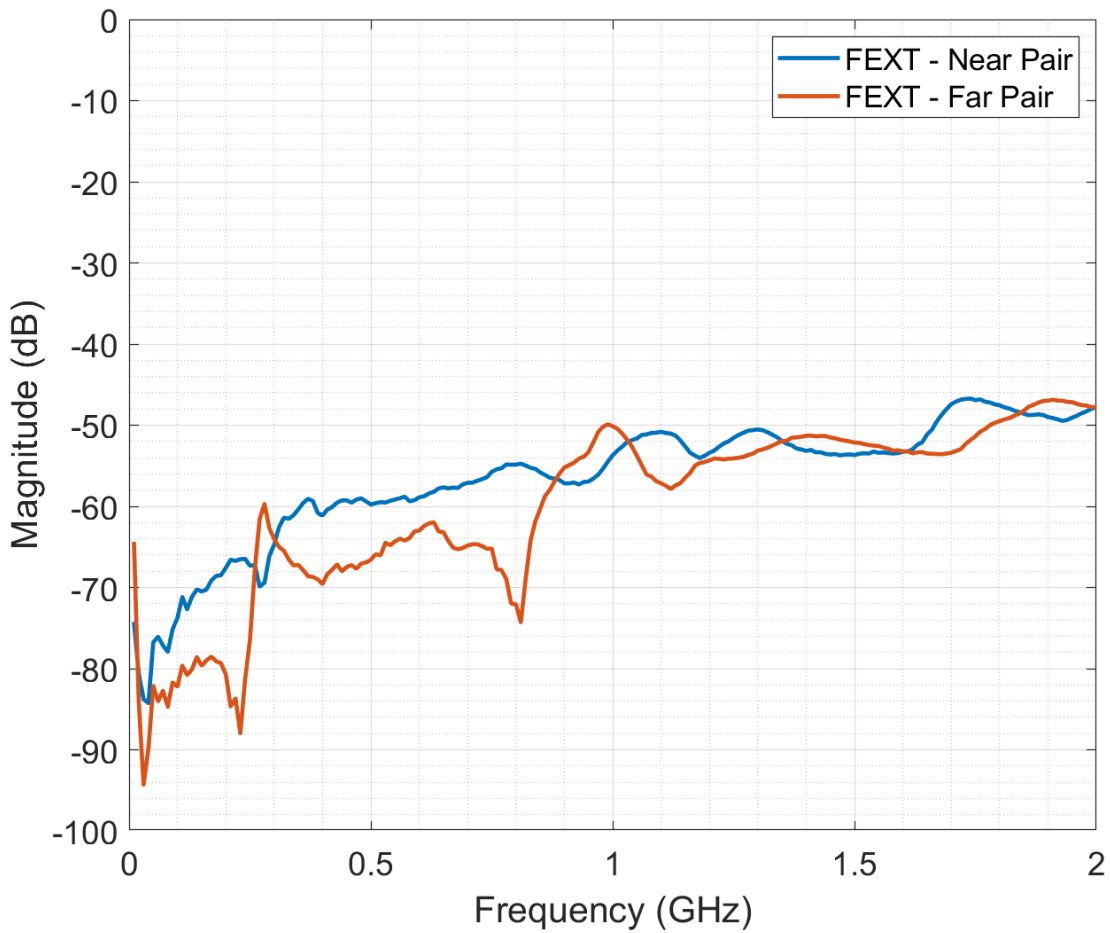


Figure 31. FEXT – Wired Connector GHSM (15E) Mated Pair

8.2. Time Domain Analysis – Wired Connector GHSM (15E) Mated Pair

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal’s rising edge. Rise times of 100ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
100	3.5
200	1.75

Table 1. Bandwidth to Rise Time Relationship

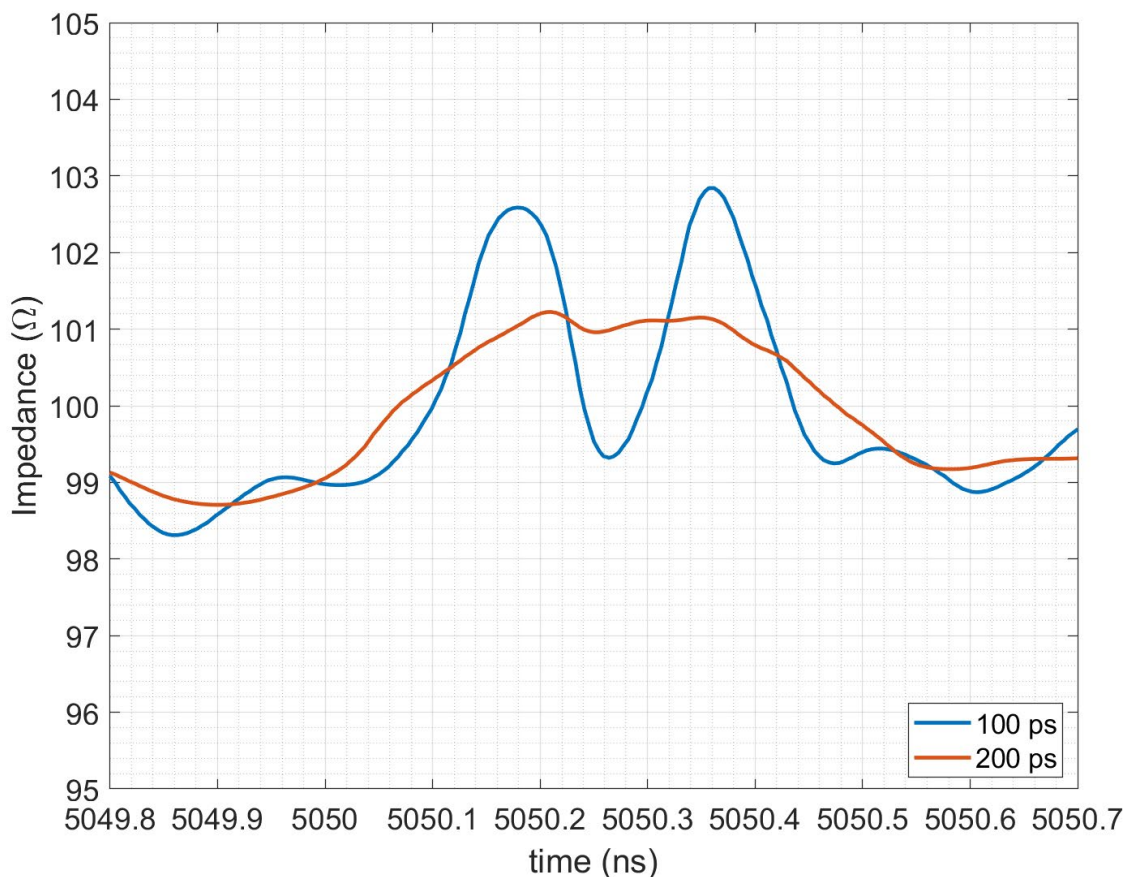


Figure 32. TDR – Wired Connector GHSM (15E) Mated Pair

9. Performance – FeedThru Connector

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

9.1. Frequency Domain Analysis

9.1.1. Insertion Loss – FeedThru Connector Pair

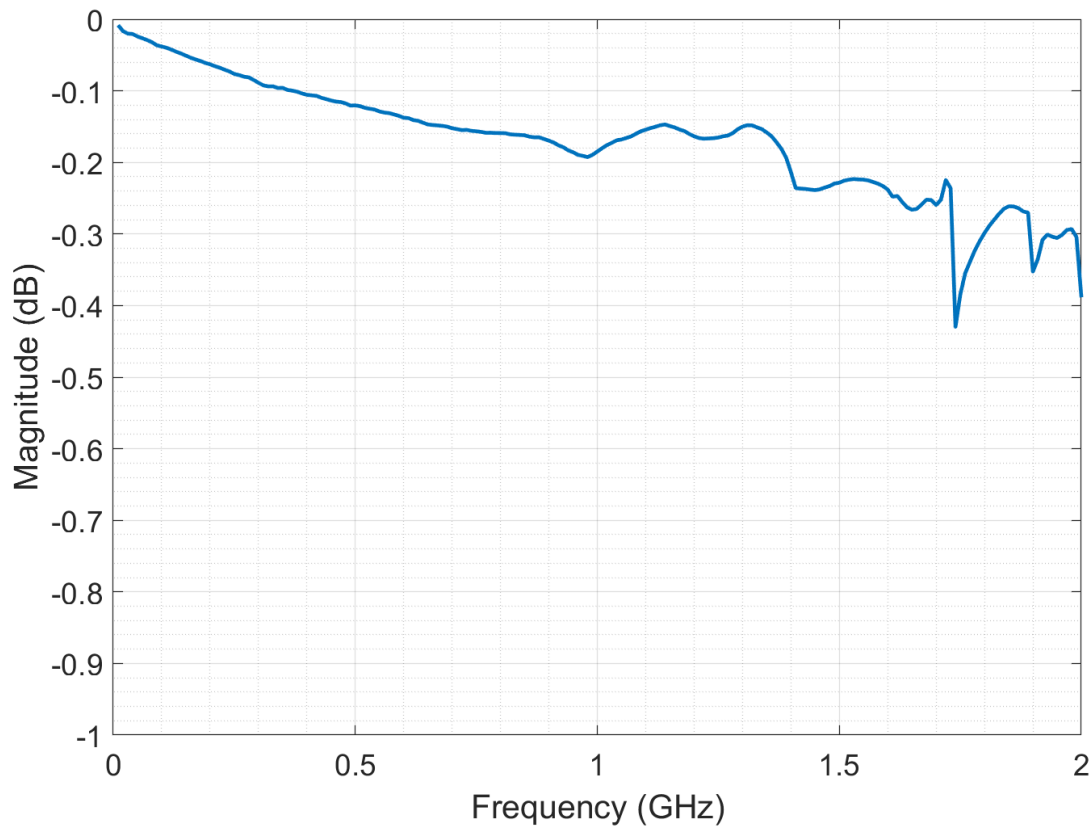


Figure 33. Insertion Loss – FeedThru Connector

9.1.2. Return Loss – FeedThru Connector

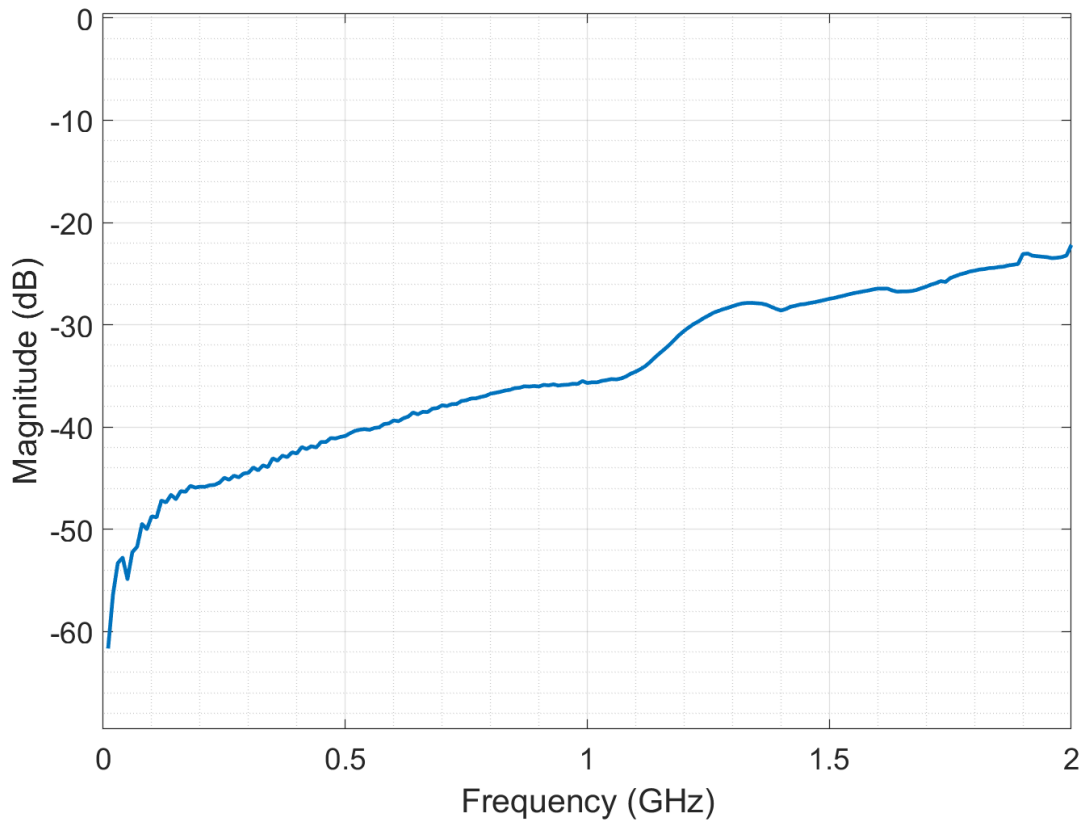


Figure 34. Return Loss – FeedThru Connector

9.1.3. NEXT – FeedThru Connector

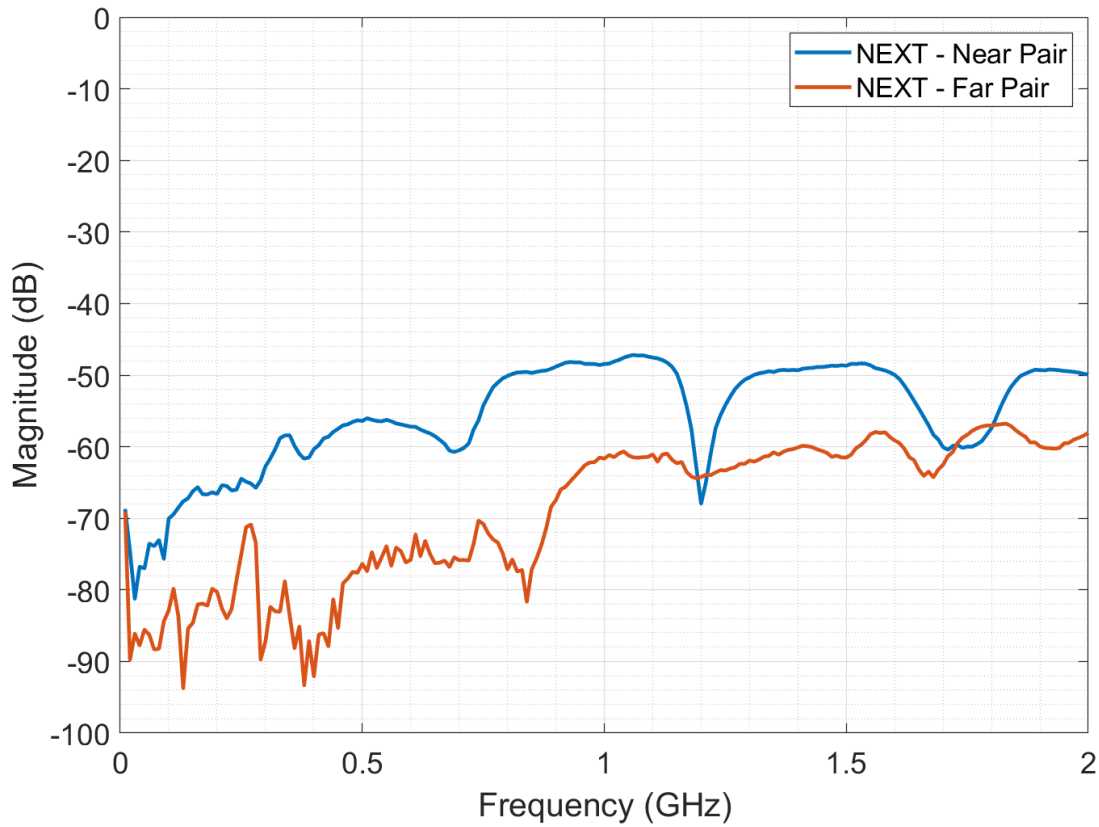


Figure 35. NEXT – FeedThru Connector

9.1.4. FEXT – FeedThru Connector

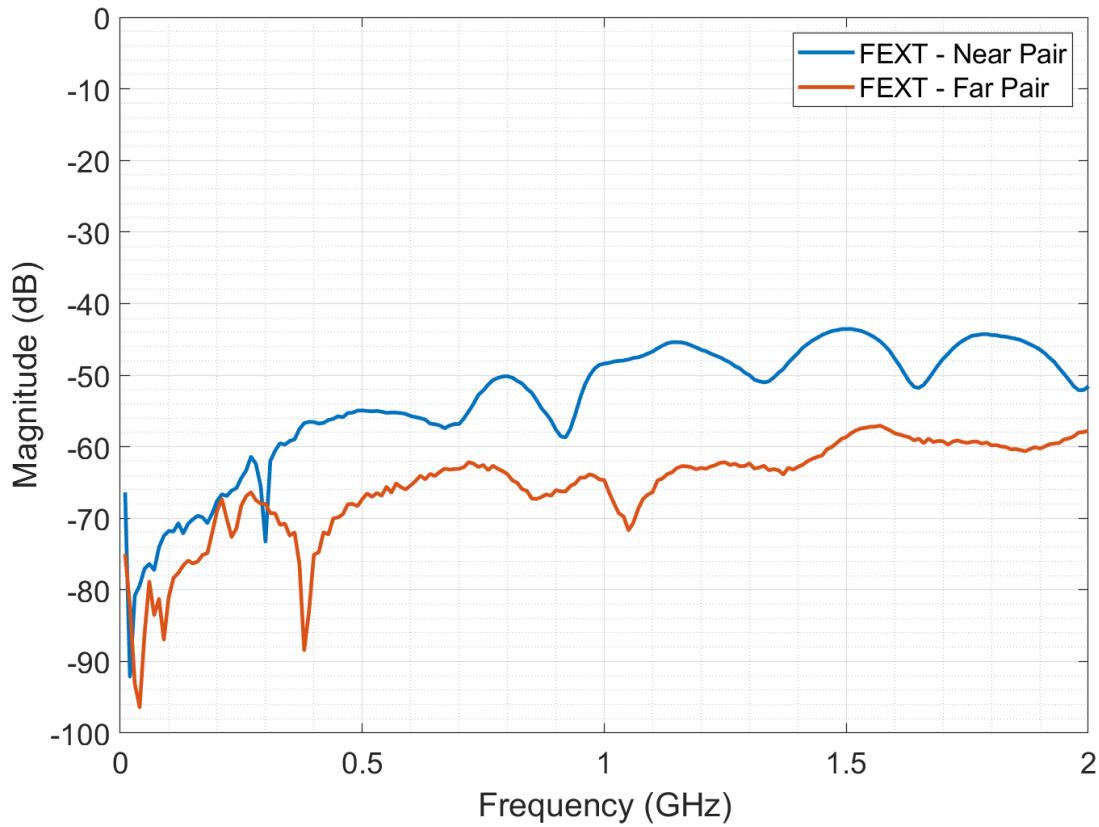


Figure 36. FEXT – FeedThru Connector

9.2. Time Domain Analysis – FeedThru Connector

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal’s rising edge. Rise times of 100ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
100	3.5
200	1.75

Table 1. Bandwidth to Rise Time Relationship

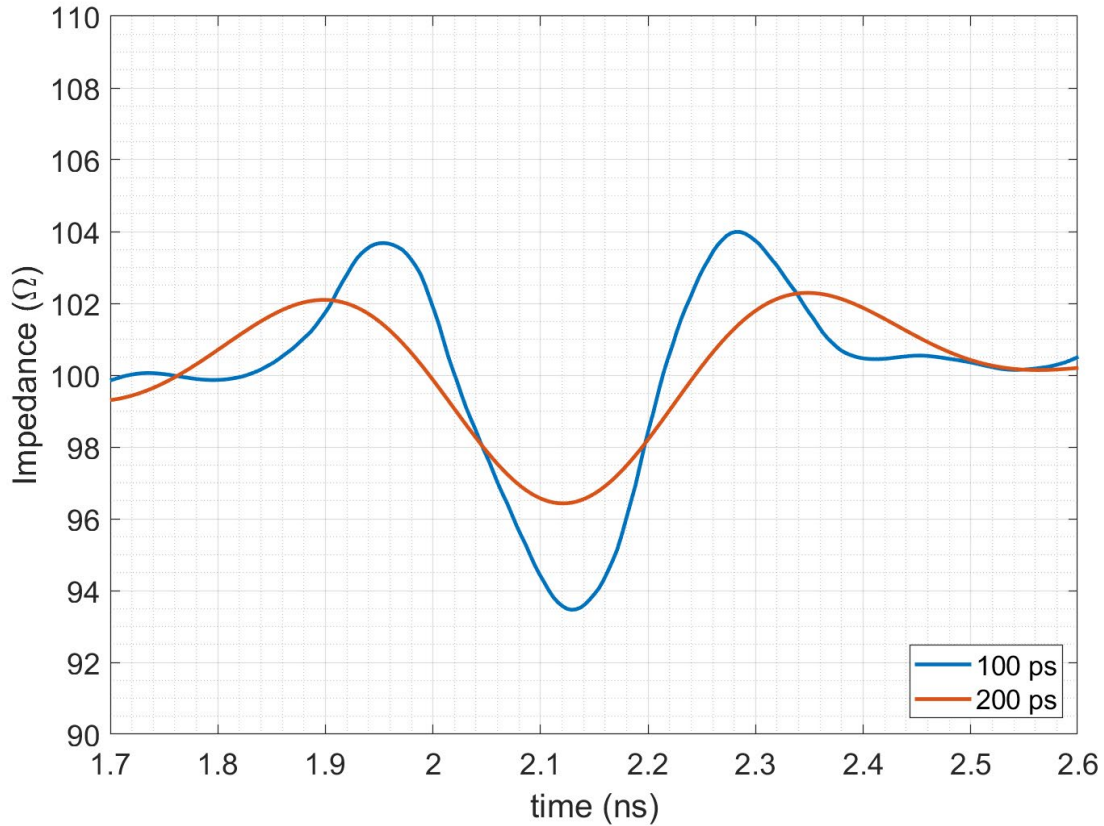


Figure 37. TDR – FeedThru Connector

10. Performance – Sav-Con Connector

This section includes both frequency and time domain results. Test fixture PCB loss has been de-embedded to show the performance of the assembly only.

10.1. Frequency Domain Analysis

10.1.1. Insertion Loss – Sav-Con Connector Pair

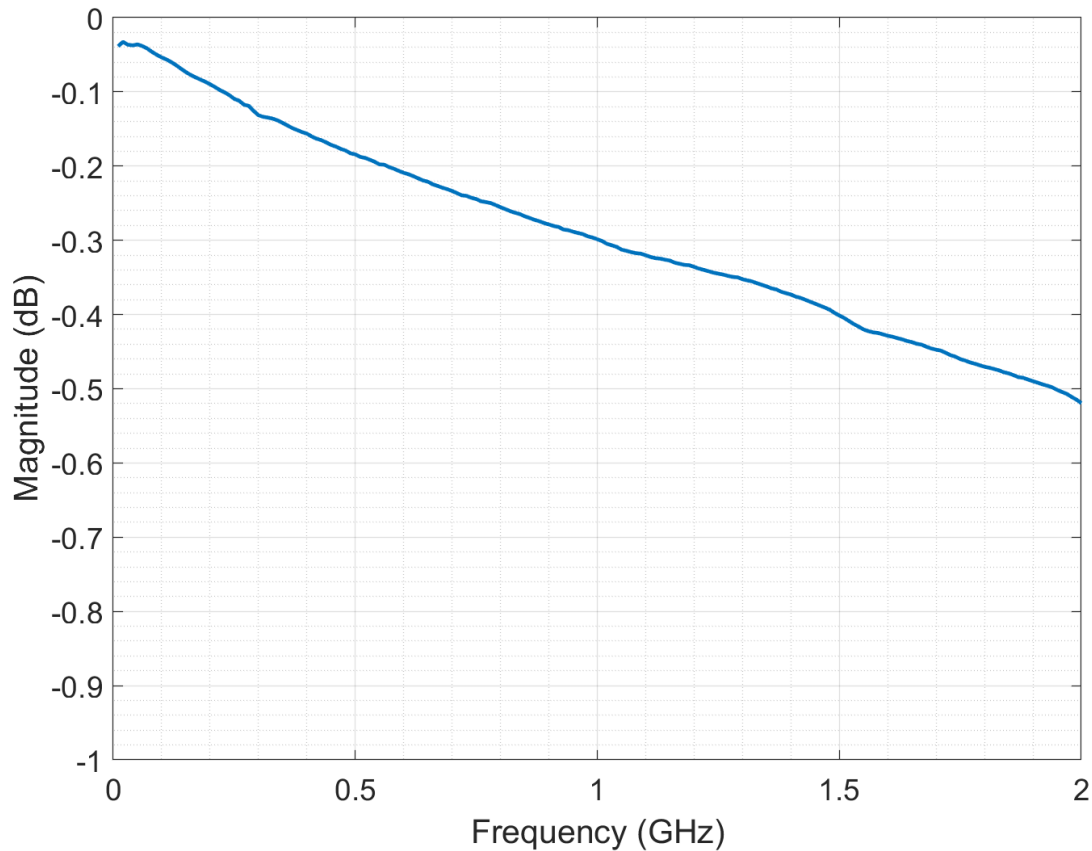


Figure 38. Insertion Loss – Sav-Con Connector

10.1.2. Return Loss – Sav-Con Connector

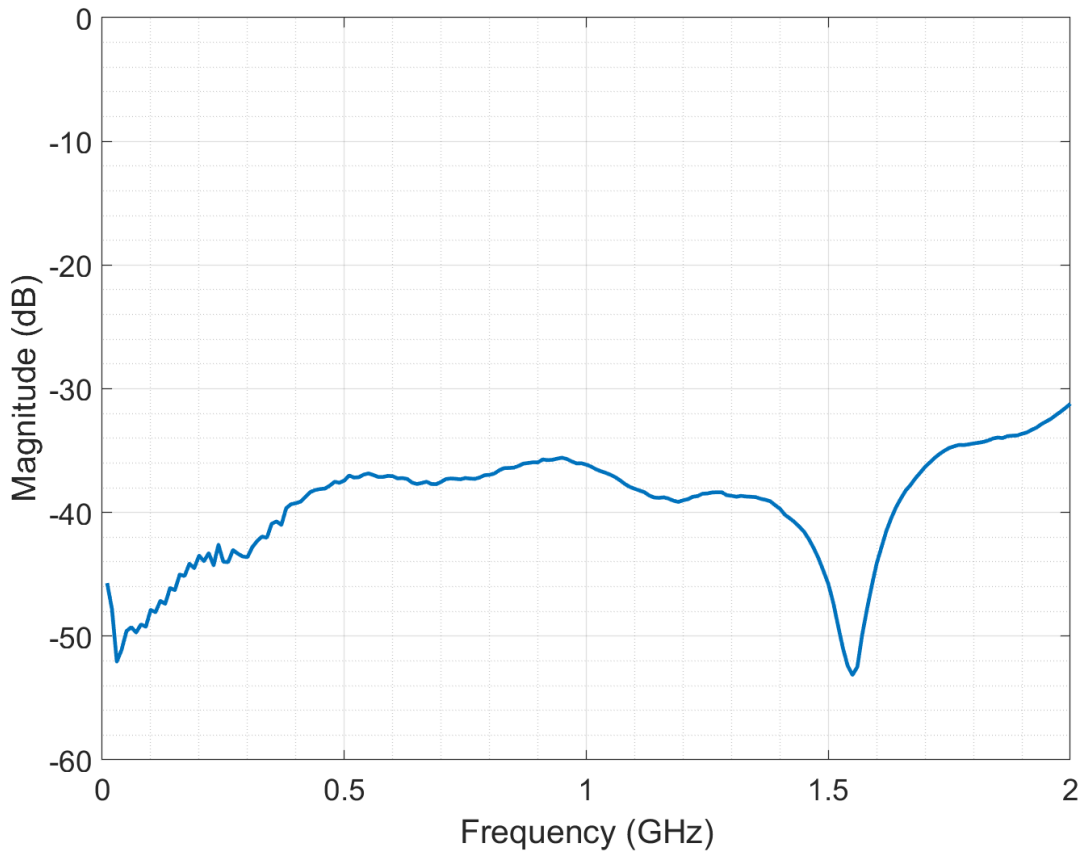


Figure 39. Return Loss – Sav-Con Connector

10.1.3. NEXT – Sav-Con Connector

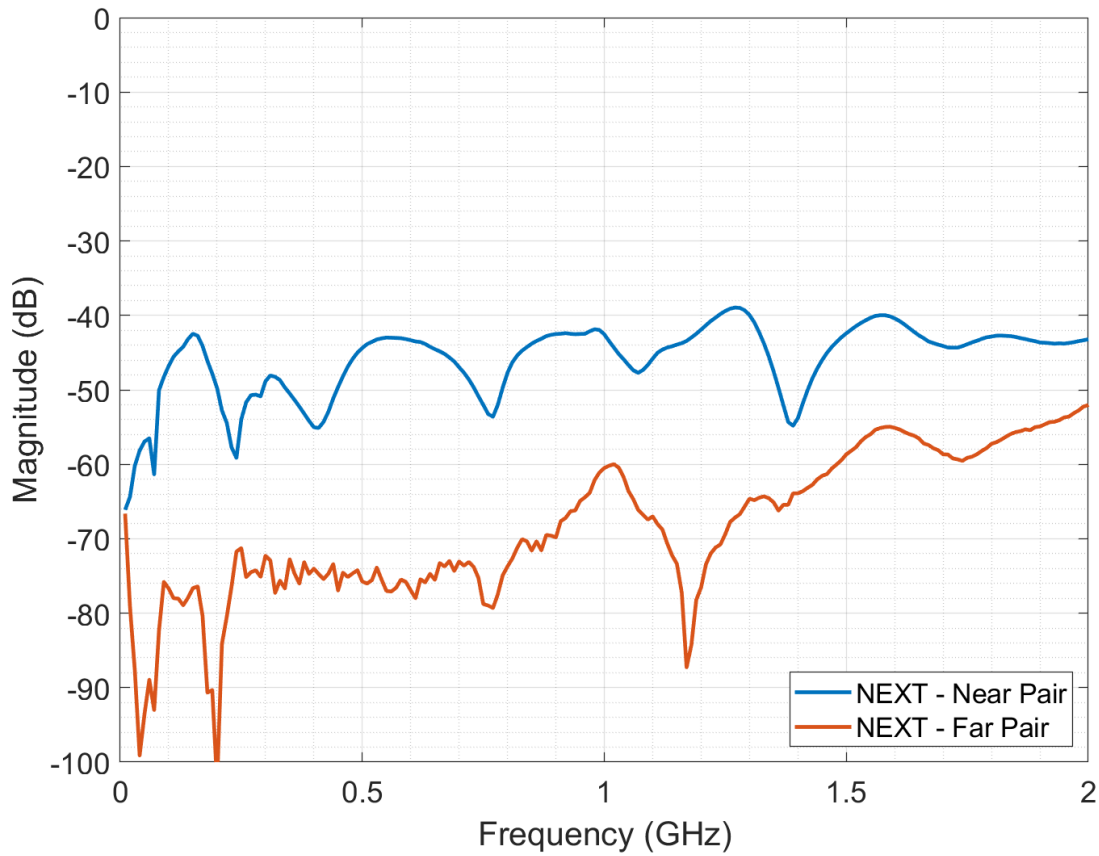


Figure 40. NEXT – Sav-Con Connector

10.1.4. FEXT – Sav-Con Connector

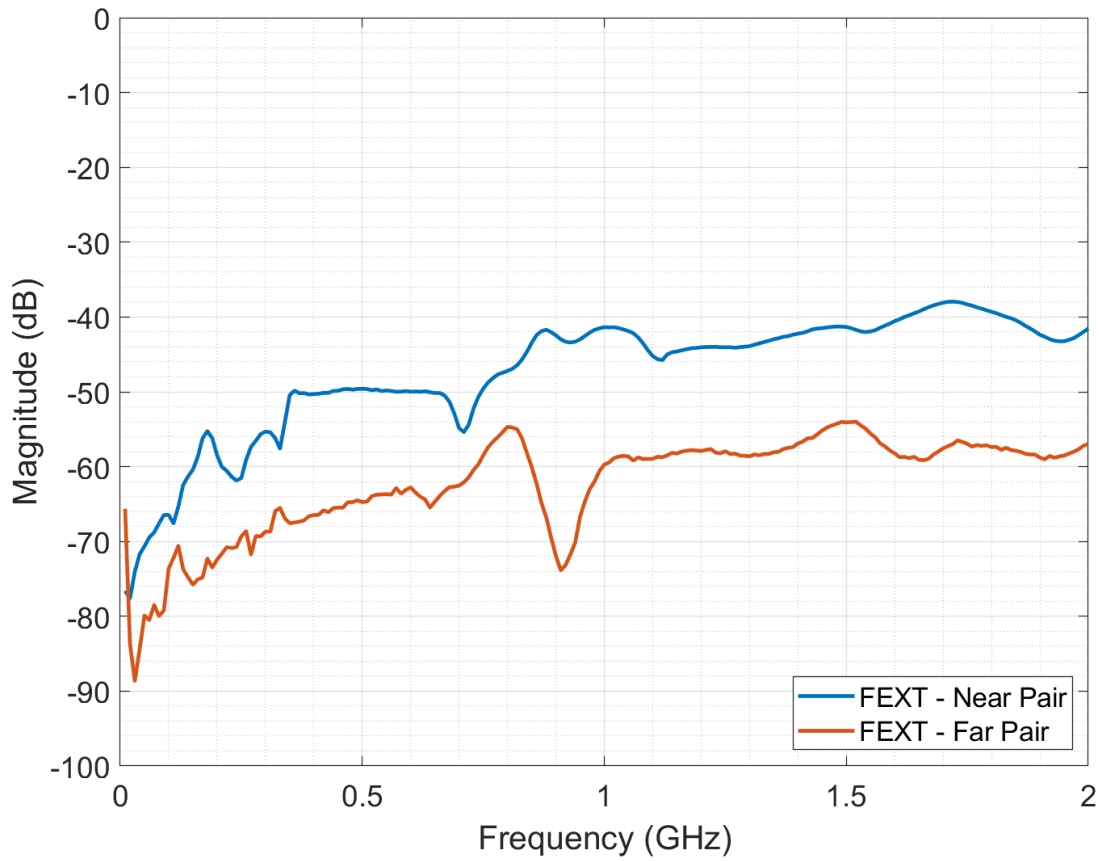


Figure 41. FEXT – Sav-Con Connector

10.2. Time Domain Analysis – Sav-Con Connector

Time domain data was generated in real time using a Tektronix DSA8300 Digital Serial Analyzer. Graphs for each test cable and pair configuration are shown below for various rise times. Rise time is defined at 10% to 90% of the signal’s rising edge. Rise times of 100ps and 200 ps were used. The following table shows the relative bandwidth, BW, for a given TDR test step rise time, t_r .

t_r (ps)	BW(GHz)
100	3.5
200	1.75

Table 1. Bandwidth to Rise Time Relationship

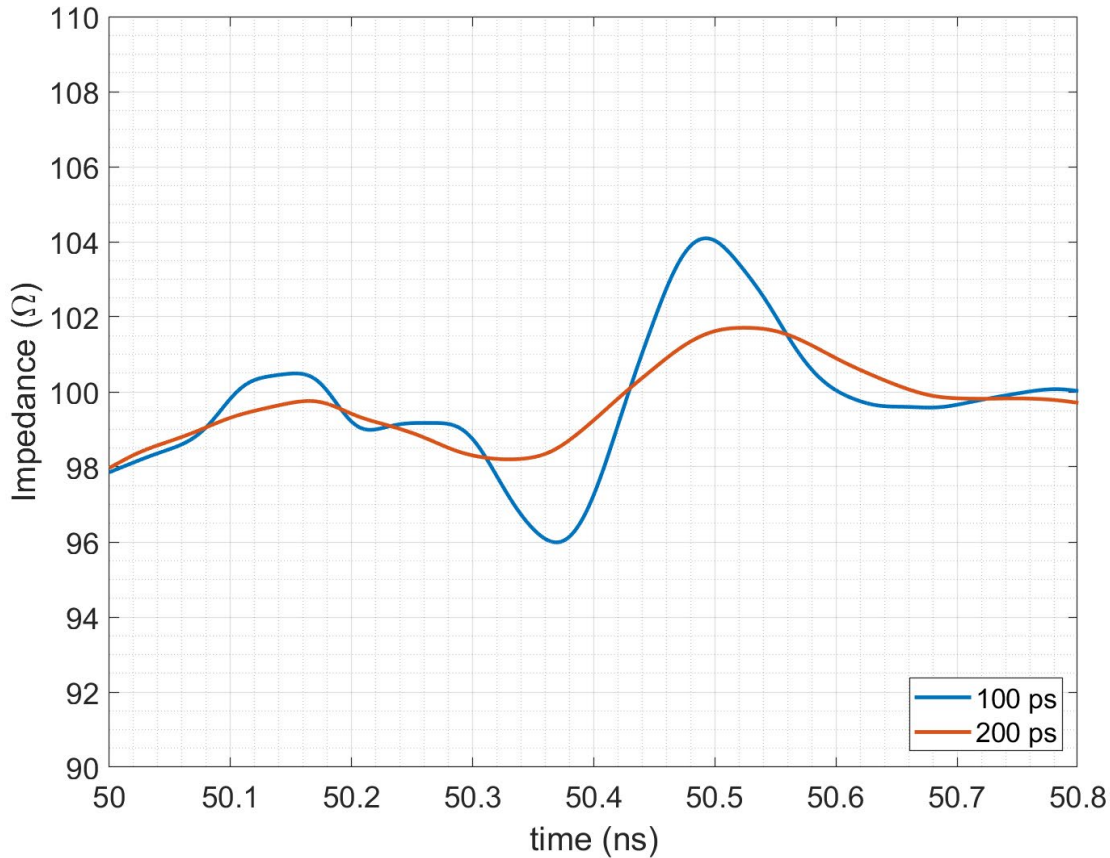


Figure 42. TDR – Sav-Con Connector